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Low-power Adiabatic Logic Circuit: Simulation and Energy Dissipation Comparison

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SUMMARY This paper investigates the design approaches of low-power adiabatic logic gates in terms of energy dissipation associated with the input transition. A computer simulation using SPICE is carried out on several inverter circuits implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the logic gates. The dissipation characteristics are also compared at the different load capacitance values.

key words: *adiabatic logic*

Presentation content

- 2008/09/26 : Circuit Simulation and Energy dissipation at different C
- 2008/10/03 : Circuit Simulation and Energy dissipation at different C (continue)
- 2008/10/10 : Circuit Simulation with new diagrams
- 2008/10/17 : More Circuit Simulation and Energy Dissipation comparison
- 2008/10/27 : Simulation using new MOS parameters and updated Energy Dissipation comparison
- 2008/10/31 : Draft for Technical Report of IEICE
- 2008/11/07 : Draft for Technical Report of IEICE (con't)
- 2008/11/14 : Mastering Basic LSI (Course Report
- 2008/11/21 : QSERL, APDL, REL and new inverter circuits simulation and energy dissipation comparison

1. Evaluated circuits and results

In this presentation, diode based inverter circuits have been evaluated.

1.1 QSERL

In quasi-static energy recovery logic (QSERL) [1], nodes are not neccessarily charging and discharging every clock cycle which reduces the node switching activities significantly. The lower switching activityreduces energy dissipation. QSERL can be converted from static CMOS circuits without huge modification on the circuit complexity and transistor overheads. From the simulation, it shows that QSERL dissipates 1.87 pJ in energy, which is about 44

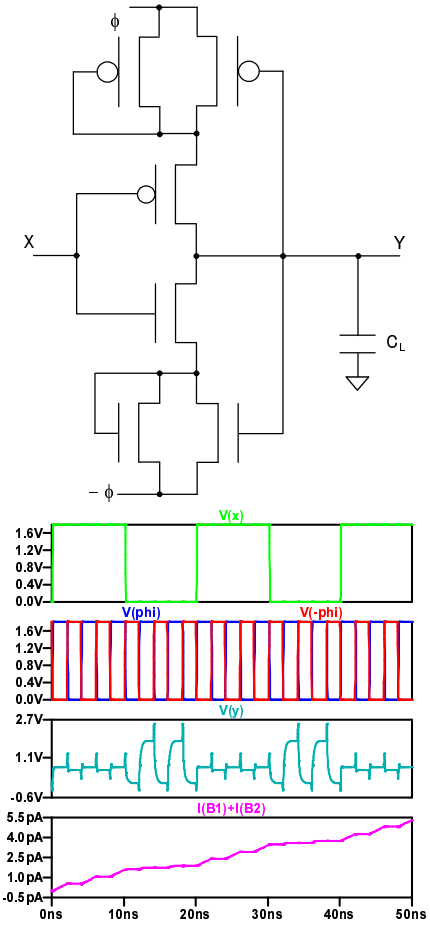

Fig. 1 Quasi-static energy recovery logic (QSERL) circuit diagram and waveforms

1.2 APDL

The next circuit to be investigated is adiabatic pseudo-domino logic family (APDL) [2]. It provides a higher frequency performance in excess of 1Ghz with simple clock supplies. From the simulation the energy dissipation for APDL inverter is 2.61 pJ, which is about 22% less than conventional static CMOS.

1.3 REL

Recovery energy logic circuit (REL) [3] has been examined. From the simulation result REL is not yet functioning as an inverter. This circuit will be discussed in the next presentation.

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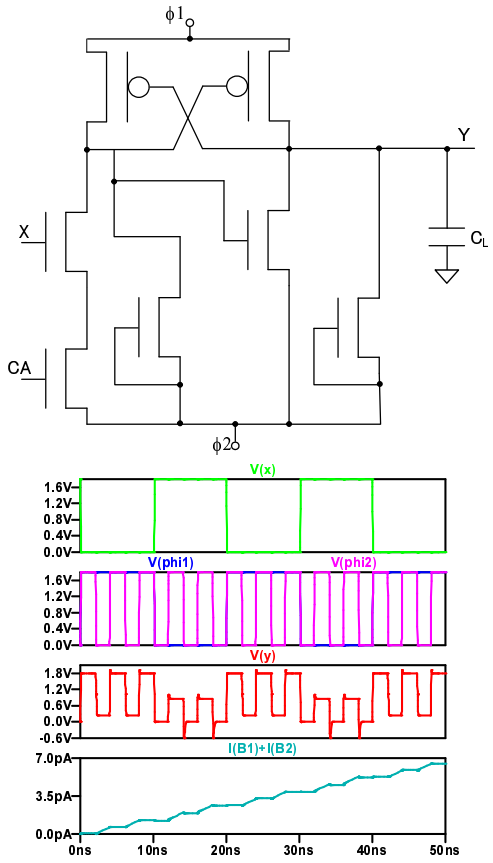

Fig. 2 Adiabatic pseudo-domino logic (APDL) circuit diagram and waveforms

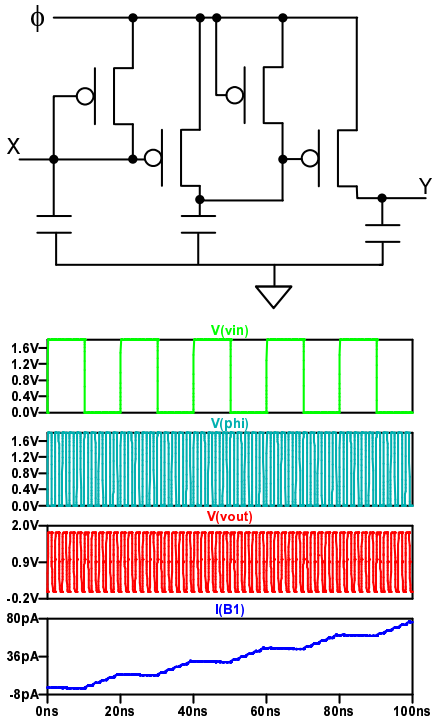

Fig. 3 Recovery energy logic (REL) circuit diagram and waveforms

1.4 New circuit

For the new proposed circuit, it is a diode based with 2 clocked pulse signal inversed to each other. The concept is more like 2 ADL circuits combined. The dioded used as the charging and discharging. From the simulation, the energy dissipation is still 3.73 pJ, which is a little higher than CMOS logic. Further investigation will be carried out to this circuit.

Table 1 Comparison of Energy Dissipation

Adiabatic Logic	Energy(pJ/cycle)	Gates	Driving Pulse
ADL	0.035	4	4
2n-2n2D	0.095	6	1
ADCL	0.133	4	1
1n-1p SLCR	0.34	4	1
HCnMOS	0.60	5	2
2PADCL	0.77	4	2
1n-1p SLP	0.86	2	2
QSERL	1.87	6	2
1n-1p quasi	2.04	2	1
APDL	2.61	7	2
CMOS	3.33	2	1
2n2p-2n	3.45	6	1
ECRL	3.61	4	1
New Circuit	3.73	5	2
2n-2n2p quasi	5.69	6	1

2. Discussion and conclusion

From this investigation, QSERL and APDL inverter circuits demonstrate a function as an inverter based on the waveforms of the simulation result. The energy dissipation is about 44% and 22% less than conventional static CMOS logic. However, REL is still not showing a function as an inverter therefore will need further investigation. New proposed circuit has been drafted with concept similar to ADL and 2n2n2D circuits. Preliminary result shows about 3.73 pJ of energy dissipated from this new proposed inverter circuit.

References

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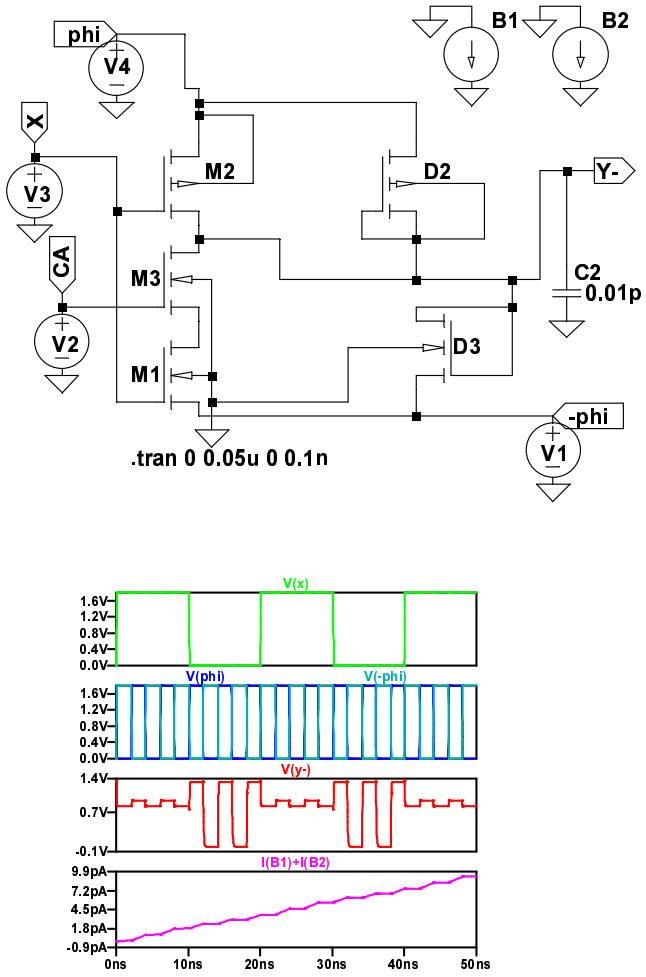

Fig. 4 Recovery energy logic (REL) circuit diagram and waveforms