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Low-power Adiabatic Logic Circuit: Simulation and Energy Dissipation Comparison

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SUMMARY This paper investigates the design approaches of low-power adiabatic logic gates in terms of energy dissipation associated with the input transition. A computer simulation using SPICE is carried out on several inverter circuits implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the logic gates. The dissipation characteristics are also compared at the different load capacitance values.

key words: *adiabatic logic*

Presentation content

- 2008/09/26 : Circuit Simulation and Energy dissipation at different C
- 2008/10/03 : Circuit Simulation and Energy dissipation at different C (continue)
- 2008/10/10 : Circuit Simulation with new diagrams
- 2008/10/17 : More Circuit Simulation and Energy Dissipation comparison
- 2008/10/27 : Simulation using new MOS parameters and updated Energy Dissipation comparison
- 2008/10/31 : Draft for Technical Report of IEICE
- 2008/11/07 : Draft for Technical Report of IEICE (con't)
- 2008/11/14 : Mastering Basic LSI (Course Report
- 2008/11/21 : QSERL, APDL, REL and new inverter circuits simulation and energy dissipation comparison
- 2008/11/28 : Presentation 1st draft for IEICE-ICD Dec 12,2008
- 2008/12/19 : New proposed adiabatic logic inverters

1. Introduction

In integrated circuits, about 70-80% is the dynamic power consumption. It means that the energy is mostly dissipated during the transition state of the transistors. The purpose of adiabatic switching circuit is to reduce the energy (heat) lost. This could be done if the transformation takes palce sufficiently slowly. Another way is to improve energy conservation by recycling the charge. In contrast to an adiabatic circuit, a conventional CMOS logic does not recycle the charge. Just before the state transition occur, a relatively large current flows through PMOS and NMOS transistors and the energy stored into the capasitive node is lost during the discharge. In our previous comparison study, most of the adiabatic inverter circuits show a lower energy dissipation comapared to conventional CMOS logic. Furthermore, diode based circuits demonstrate a lower energy dissipation compared to transistor based. This is mostly due to the diode threshold voltage, Vt . During charging and discharging to the load capacitor, $(1/2)C(V_{dd} - V_t)^2$ dissipated as heat each time compared to $(1/2)C(V_{dd})^2$ when charging and discharging through transistor. Then, the current can be rectified using diodes. From the other experiment, diode based circuits also show a lower energy dissipation when increase the load capacitance value. Based on above results, we propose a few new circuits.

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2. New proposed adiabatic circuit

In this presentation a few modfied and new adiabatic circuits will be proposed based on the review and simulation results done before.

2.1 Modified 2PADCL

The difference with 2PADCL is the position of the diodes. As shown is Fig.2.1, when charging, the current will flow to the diodes from the pMOS transistor. When discharging, it will flow via a diode first before the transistor. For the diodes, W/L is 0.8μm and 4μm.

2.2 2P-1p1n1D

This circuit uses only 1 diode W/L is 0.8μm and 4μm for discharging.

2.3 2P-1p1n2D

This circuit uses 1 diode parallel to pMOs for charging when the input is HI and another diode that is put series with the nMOS for discharging.

2.4 2P-1pD1n1D

The difference with 2p-1p1n2D is that the diode used as discharging is near to the driving pulse. This design is useful when calculating the location of nMOS tree.

2.5 1p2D

For this circuit, only 1 pMOS and 2 diodes are used.

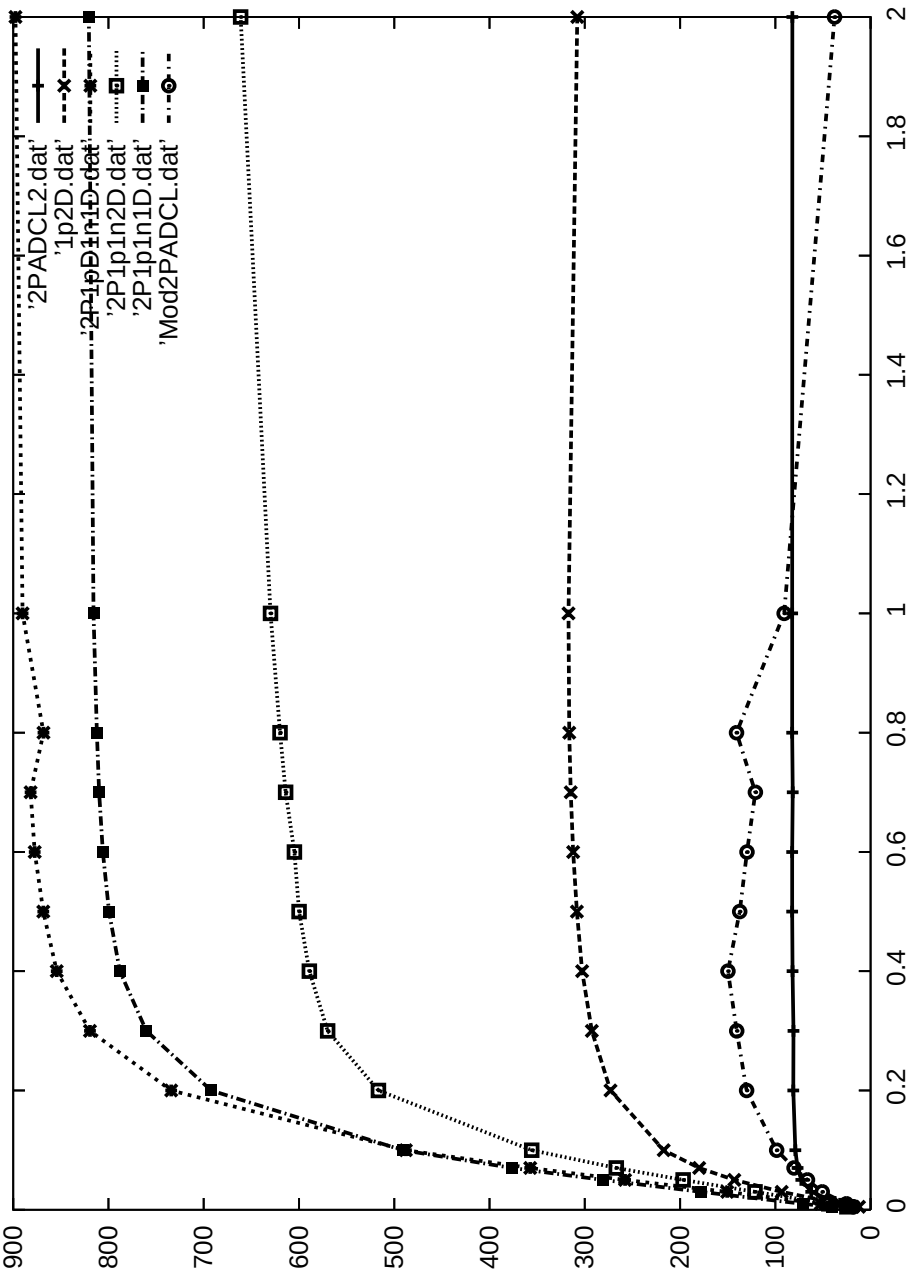

Fig. 6 Energy dissipation comparison in adiabatic circuits at different load capacitance value

3. Results

3.1 Discussion and Conclusion

A few adiabatic logic inverter circuits have been proposed based on the relatively low energy dissipation 2PADCL circuit. The modified 2PADCL shows a better result from this simulation. It also demonstrate a good characteristic when load capacitance increased.

Table 1 Comparison of Energy Dissipation

Adiabatic Logic	Energy(fJ/cycle)	Gates	Driving Pulse
Mod 2PADCL	25.80	4	2
1n2D	32.12	3	1
2PADCL	31.97	4	2
2P1p1n2D	43.86	4	2
2P1pD1n1D	49.28	4	2
2P1p1n1D	68.96	3	2

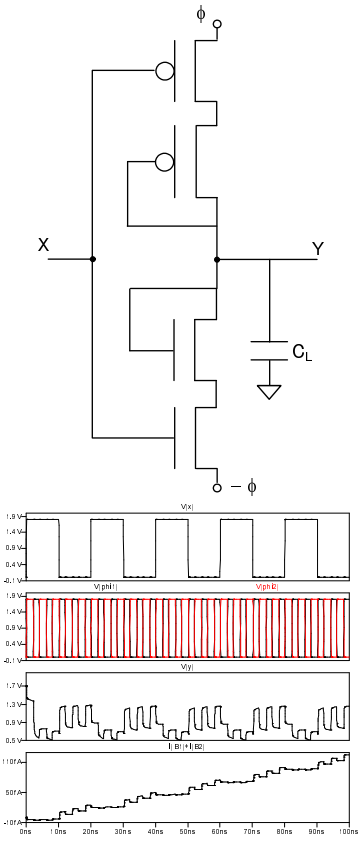

Fig. 1 Modified 2PADCL inverter circuit diagram and waveforms

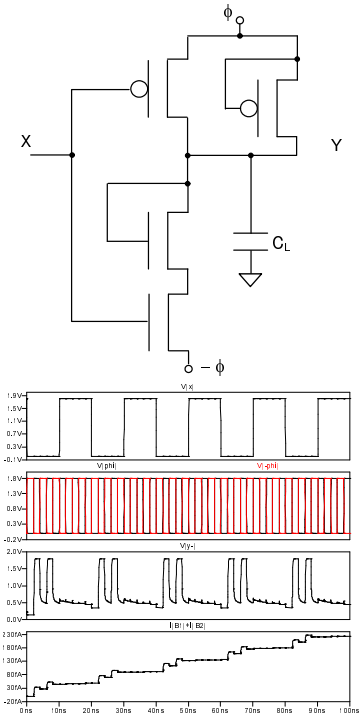

Fig. 3 2P1p1n2D inverter circuit diagram and waveforms

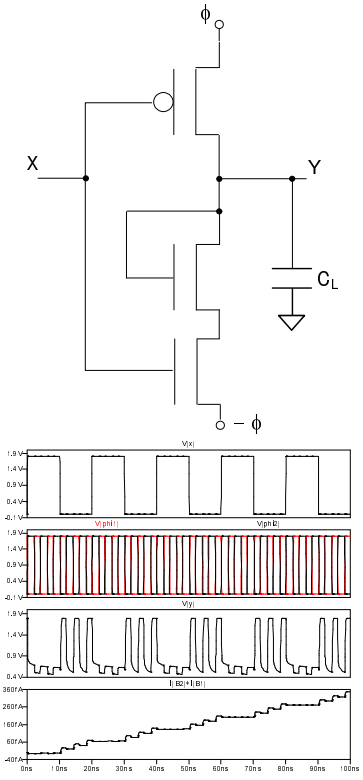

Fig. 2 2P1p1n1D inverter circuit diagram and waveforms

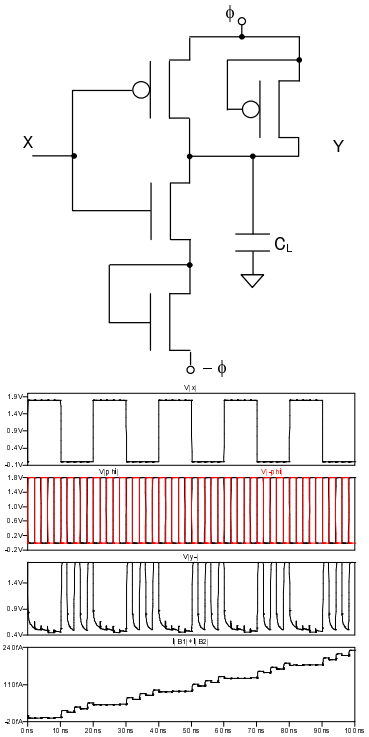

Fig. 4 2 Phase 1p-1D1n1D inverter circuit diagram and waveforms

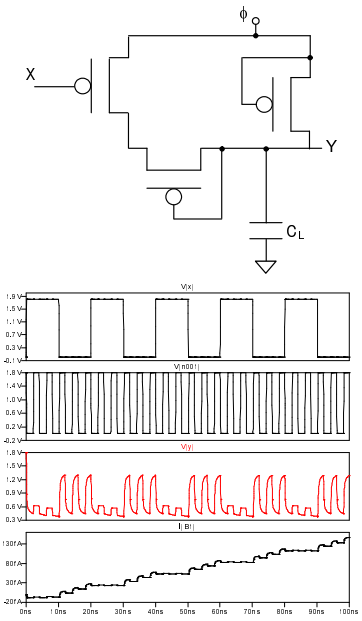

Fig. 5 1p2D inverter circuit diagram and waveforms