4-bit Ripple Carry Adder (RCA) of 2PASCL : comparison with static CMOS

Nazrul Anuar

Graduate School of Eng., Gifu University

Abstract

The paper presents a new quasi energy recovery logic family that uses two complementary split-level sinusoidal power supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) is using the principle of adiabatic switching. It has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL logic gates implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. For an inverter and four-inverter chain, it shows that 2PASCL can save 82.6% and 56.9% of energy respectively over static CMOS logic at transition frequency of 100MHz.

1 Introduction

In the previous simulation, we redesign the exclusive-OR(XOR) of 2PASCL which consist of 15 transistors including the inverters and diodes and compared with exclusive-OR CMOS which consist only 6 transistors. Then, we again combine it with the NAND circuit to create full adder (FA) combination circuit. Comparison with CMOS FA in term of energy dissipation is carried out. 1-bit full adder of 2PASCL shows 21.7% lower energy dissipation at input frequency of 16.7 MHz compared with static CMOS. Next, we introduce the 4-bit ripple carry adder (RCA) of 2PASCL by showing the output waveforms.

In this paper, we select the design of XOR of 2PASCL which shows the lowest energy dissipation performance. Then, we demonstrate the result of FA of 2PASCL and compared with static CMOS. Then, we arrange 4 FAs to create 4-bit ripple carry adder (RCA). The output results and the comparison with static CMOS at transition frequencies of 10 to 100 MHz is carried out.

2 Simulation and results

By using split level driving voltage sinusoidal ranging from 0 to 1.8V, simulations of new exclusive-OR 2PASCL is carried out. We simulate the circuit by changing the location of the diode used to recycle the charges. We also connect the inverters nMOS to the diodes. The lowest energy dissipation provided from the circuit which schematic is in Fig. 2. Next, we simulate the XOR of CMOS shown in Fig. 3 for adiabatic switching by adding the split level sinusoidal driving voltage and diodes to recycle the charges. However, the circuit does not show an adiabatic operation and the energy dissipation is high. Therefore, schematic in Fig. 3 is only used for static CMOS XOR. Bulks are connected to ϕ and $\overline{\phi}$. The circuit condition is as shown in Table 1.

By using this new schematic, full adder (schematic as in Fig. 1), which consist of exclusive-OR and NAND logics, is simulated for 2PASCL and CMOS. The results for full adder (circuit layout as in Fig. 8) are shown in Fig. 4 and Fig. 5. 4 FAs are used to simulate ripple carry adder which layout of the 2PASCl version is as shown in Fig. 10. The results for ripple carry adder are shown in Fig. 6 and Fig. 7 for CMOS. The comparison of the energy dissipation for the transition frequency of 10 MHz with conventional static CMOS logic with V_{dd} of 1.8V is shown in Table 2. From the results, 2PASCL with split level sinusoidal clocking voltage gives a significant lower energy dissipation compared to conventional static CMOS for 4-bit ripple carry adder even though higher for single full adder (FA). 2PASCL ripple carry adder (RCA) also shown a significant lower energy dissipation when transition frequency simulated from 10 to 100 MHz (Fig. 9).

Table 1 Circuit data for sinusoidal and static CMOS comparison

Driving power voltage	0–1.8V
Split level	0–0.9V, 0.9–1.8V
Freq, (input: driving voltage)	1:4
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm

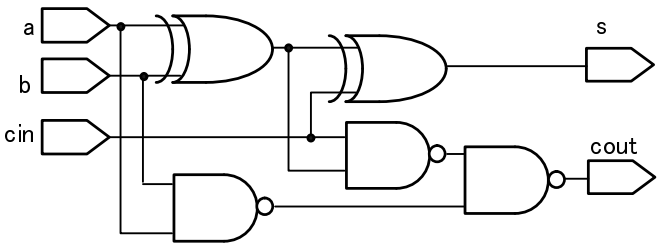

Fig. 1 Full adder.

Table 2 Energy dissipation per cycle comparison

	CMOS [μW]	2PASCL[μW]	Diff [%]
FA (@ 10 MHz)	0.917	2.207	144.68
RCA (@ 10 MHz)	98.211	22.217	-77.38

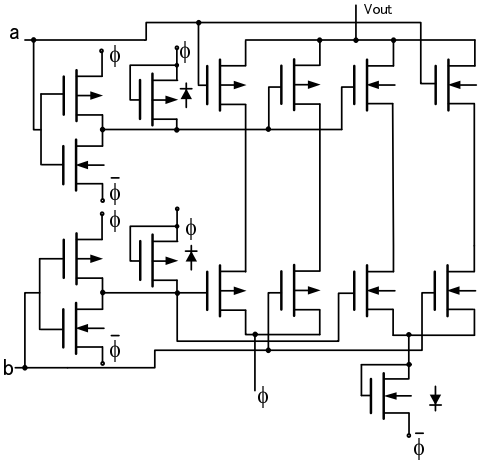

Fig. 2 Schematic for exclusive-OR of 2PASCL.

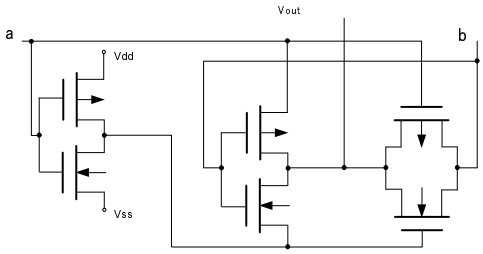

Fig. 3 Schematic for exclusive-OR of CMOS.

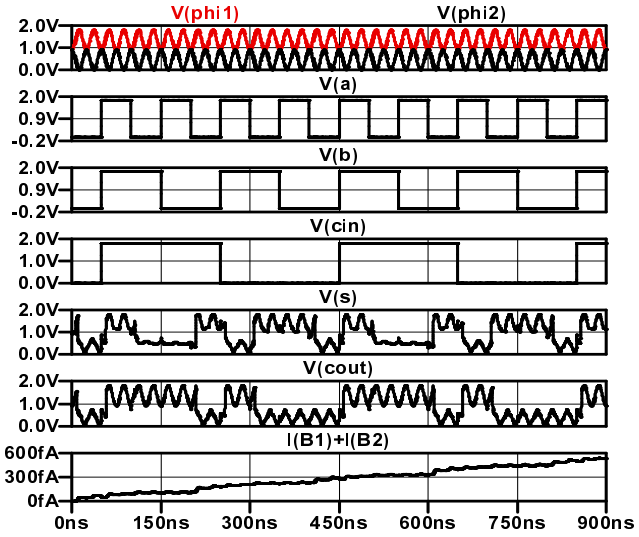

Fig. 4 Output waveforms for 1-bit full adder of 2PASCL from the simulation result.

3 Conclusion

In this simulation, 4-bit ripple carry adder (RCA) of 2PASCL shows an average of 71.5% lower energy dissipation at input frequency between 10 to 100 MHz compared to static CMOS. However further simulation need to be done to magnify the output waveforms for HIGH and LOW signals.

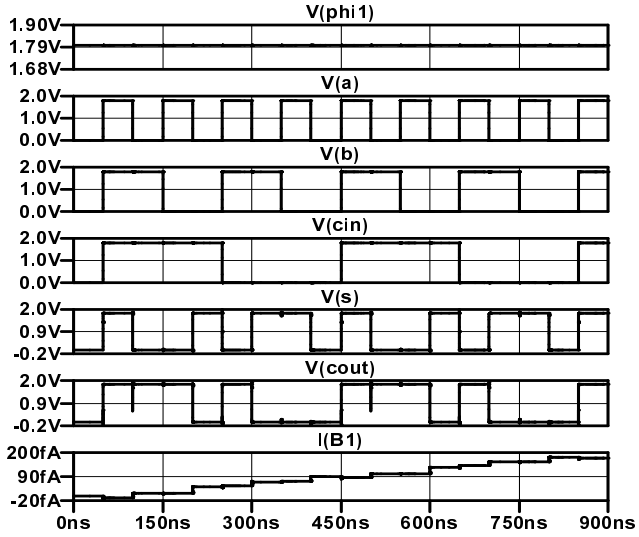

Fig. 5 Output waveforms for 1-bit full adder of CMOS from the simulation result.

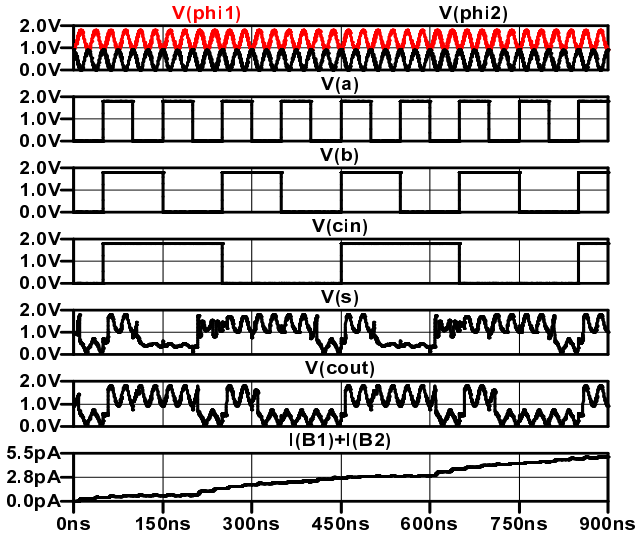

Fig. 6 Output waveforms for 4-bit ripple carry adder of 2PASCL from the simulation result.

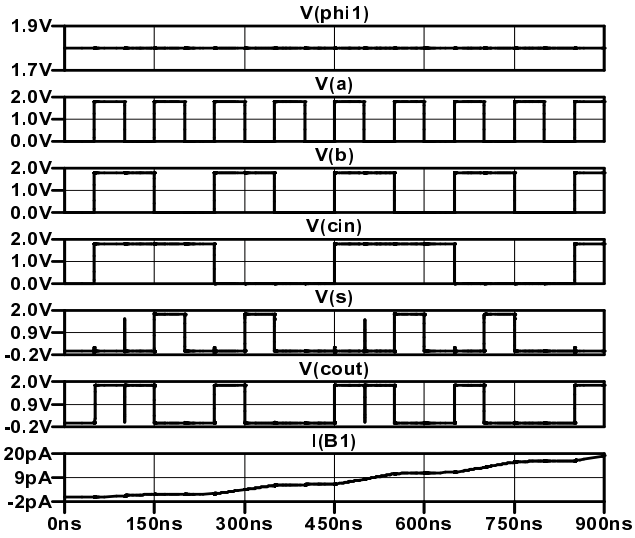

Fig. 7 Output waveforms for 4-bit ripple carry adder of CMOS from the simulation result.

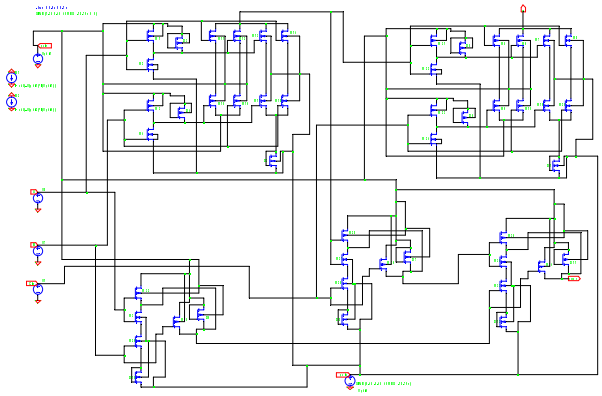

Fig. 8 Schematic of 1-bit FA of 2PASCL.

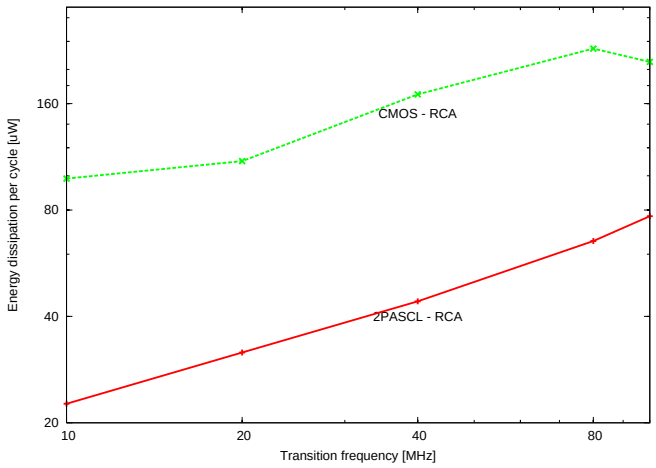

Fig. 9 Energy dissipation comparison with different transition frequency for 4-bit RCA.

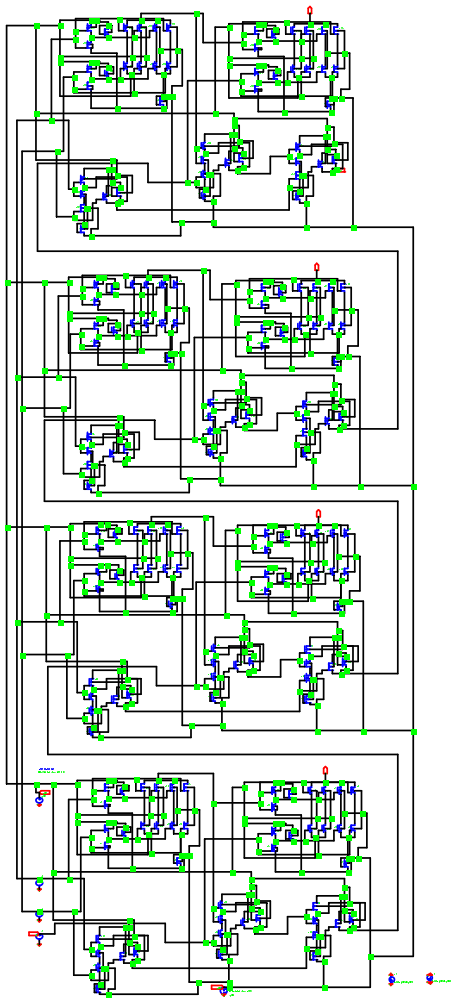

Fig. 10 Schematic of 4-bit RCA of 2PASCL