Supply clock generation (driver) circuit for 2PASCL: Hara active inductor equivalent circuit and simulation

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Abstract

The paper presents a split-level sinusoidal power supply clock generator circuit for Two-Phase Adiabatic Static CMOS Logic circuit (2PASCL). The driving of adiabatic logic requires adiabatic controlled sources of voltage. We study the clock voltage generator circuit using SPICE simulation and investigate the most suitable scheme and highest energy efficiency for the energy recovery power supply clocks.

1 Introduction

In the previous simulation, by changing the parameters, we proposed an LC resonant driver using Hara's active inductor to generate complementary split level sinusoidal wave, ϕ and $\overline{\phi}$ for 2PASCL logic circuit. The clock generator consists of four MOS-transistors Colpitts oscillator and two active inductors, which could be integrated with the logic circuit. However, we still could not generate the required 0.9 V V_{pp}. We also yet to find inductance characteristic in the simulation. Further numerical calculation and simulation will be carried out.

In this paper, we rearrange the small signal circuit and simplified circuit of Hara active inductor. Then, we calculate the inductance L.

2 Hara Active Inductor [8]

2.1 Equivalent circuit

Figures 1 and 2 show Hara's active inductor [7] and its small signal model, respectively.

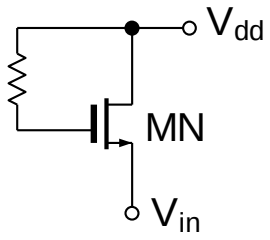

Fig. 1 Hara's active inductor.

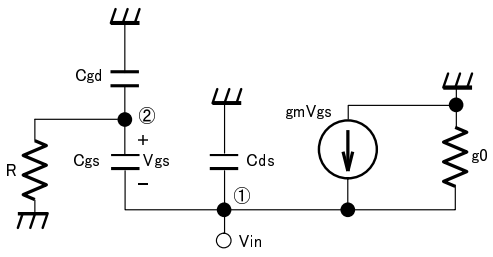

Fig. 2 Small signal equivalent circuit.

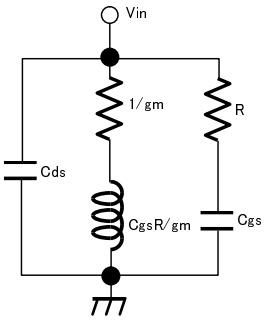

Fig. 3 Simplified Hara active inductor small signal equivalent circuit.

Fig. 2 shows small signal equivalent model. We calculate the admittance of this circuit. By using node equation at ① and ②, equations (1) and (2) are derived. Here, since $g_m \gg g_o$ and $C_{gs} \gg C_{gd}$, g_o and C_{gd} are ignored to simplify the results.

$$I_{in} + g_m V_{gs} - j\omega C_{ds} V_{in} + j\omega C_{gs} V_{gs} = 0, \quad (1)$$

$$-j\omega C_{gs} V_{gs} - \frac{1}{R}(V_{in} + V_{gs}) = 0, \quad (2)$$

tranforming above equation (1) and (2), we will get

$$I_{in} - j\omega C_{ds} V_{in} + (j\omega C_{gs} + g_m) V_{gs} = 0, \quad (3)$$

$$V_{gs} = \frac{1}{-Rj\omega C_{gs} - 1} V_{in} = 0, \quad (4)$$

by inserting eq. 4 into 3,

$$I_{in} = \left(j\omega C_{ds} + \frac{g_m}{j\omega C_{gs} R + 1} + \frac{j\omega C_{gs}}{Rj\omega C_{gs} + 1} \right) V_{in}, \quad (5)$$

and it could be rewritten as

$$I_{in} = \left(j\omega C_{ds} + \frac{1}{j\omega \frac{C_{gs} R}{g_m} + \frac{1}{g_m}} + \frac{1}{R + \frac{1}{j\omega C_{gs}}} \right) V_{in}, \quad (6)$$

From this equation, we can simplify the Hara active equivalent circuit as shown in Fig. 3

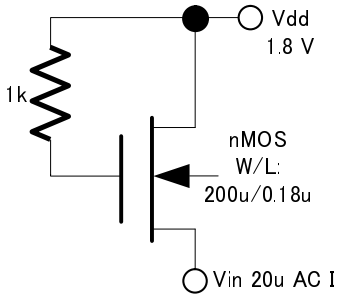

Fig. 4 Hara active inductor with values.

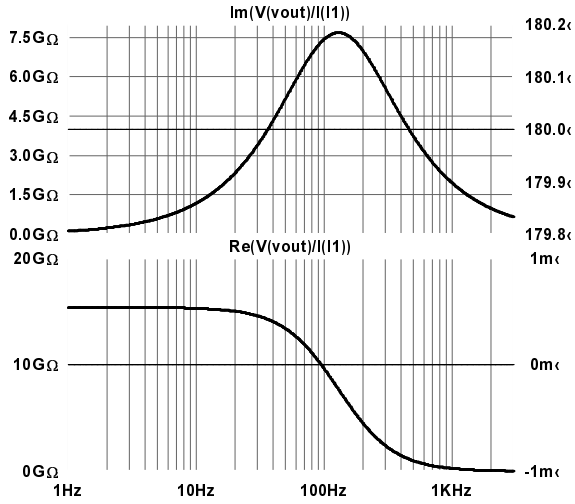

Fig. 5 Bode plot for Hara active inductor.

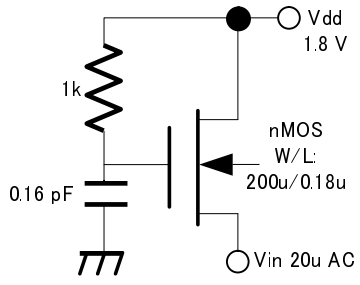

Fig. 6 Hara active inductor with capacitor.

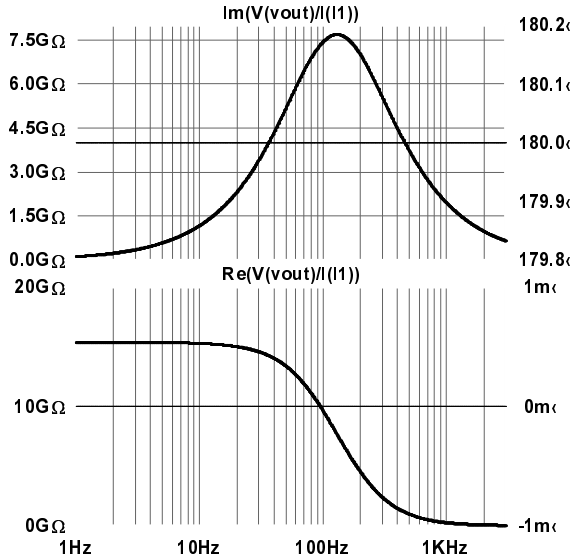

Fig. 7 Hara active inductor with capacitor.

2.2 SPICE simulation

From Fig. 5, it oscillates at 130.5 Hz and the impedance value is $Z = 7.685G\Omega$. By considering it as L impedance, we measure L as below

$$\begin{aligned} \omega L &= 7.685\ [G\Omega], \\ L &= \frac{7.685\ [G\Omega]}{2 \cdot \pi \cdot 130.5\ [Hz]}, \\ &= 9.4 \times 10^{6}\ [H]. \end{aligned} \tag{7}$$

calculating the resonant frequency, f_0 and capacitor, C by using this equation,

$$\begin{aligned} f_0 &= \frac{1}{\sqrt{LC} \cdot 2 \cdot \pi}, \\ C &= 0.16 \times 10^{-12}. \end{aligned} \tag{8}$$

by taking this L value to generate 130 Hz frequency, we simulate circuit as demonstrated in Fig. 6 with additional $C = 0.16$ pF and investigatet the Bode plot as shown in Fig. 7. The result shows that similar pattern of graph as compared with Fig. 5.

2.3 Calculation of inductance, L

The overlapped gate-source capacitance,

$$\begin{aligned} C_{gs} &= CGSO \cdot W\ (Farads) \\ &= 3.81 \times 10^{-10} \cdot 200 \times 10^{-6} \\ &= 7.62 \times 10^{-14}\ [F]. \end{aligned} \tag{9}$$

the oxide capacitance, C'_{ox} is

$$\begin{aligned} C'_{ox} &= \frac{\varepsilon_{ox}}{T_{ox}} \\ &= \frac{3.97 \cdot 8.85[aF/\mu m]}{4.22 \times 10^{-3}[\mu m]} \\ &= 8.32 \times 10^{3}\ [aF/\mu m^2]. \end{aligned} \tag{10}$$

as the hole mobility in nMOS, $\mu_n = 527.2\ [cm^2/Vs]$, the transconductance parameter, KP is

$$\begin{aligned} KP &= \mu_n C'_{ox} \\ &= 527.2[cm^2/Vs] \cdot 832 \times 10^3[aF/\mu m^2] \\ &= 43.8 \times 10^{-5}\ [A/v^2]. \end{aligned} \tag{11}$$

As for the tranconductance, g_m,

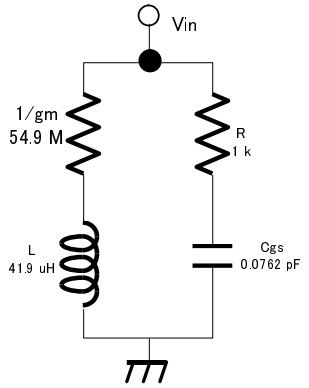

Fig. 8 Hara active inductor.

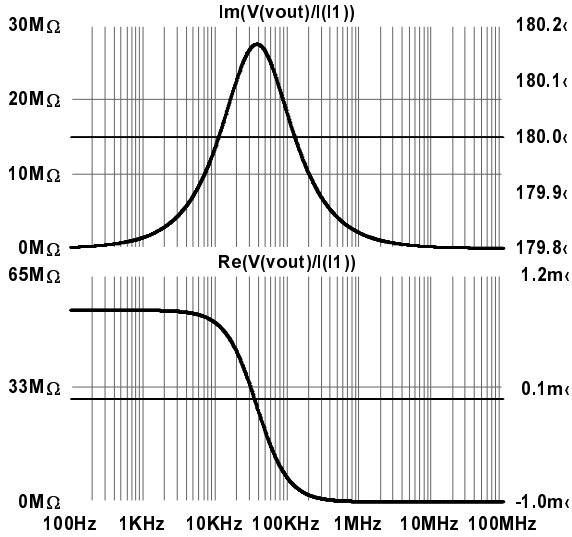

Fig. 9 Hara active inductor with capacitor Bode plot.

$$g_m = \sqrt{2\beta I_D} \quad (12)$$

$$\beta = KP \cdot \frac{W}{L} \quad (13)$$

$$g_m = \sqrt{2 \cdot 43.8 \times 10^{-5} \cdot \frac{200.0}{0.18} \cdot 3.41 \times 10^{-12}}$$

$$= 1.82.\ [\mu S]$$

from Fig. 3, $L = \frac{C_{gs}R}{g_m}$,

$$L = \frac{7.62 \times 10^{-14}\ [F] \cdot 1.0 \times 10^{3}\ [\Omega]}{1.82 \times 10^{-6}\ [S]} = 41.9\ [\mu H].$$

3 Conclusion

From the node equation of the small signal equivalent circuit, we manage to simplify the Hara active inductor circuit. Then, we input the values and simulate the result of the Bode plot. We also managed to calculate the inductance, L of the Hara active inductance circuit.

References

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