Supply clock (driver) circuit for 2PASCL: nMOS circuit characteristic prior to Hara active inductor simulation

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Abstract

The paper presents a split-level sinusoidal power supply clock circuit for Two-Phase Adiabatic Static CMOS Logic circuit (2PASCL). We investigate the most suitable scheme which provide the highest efficiency for energy recovery power supply clocks using SPICE simulation.

1 Introduction

In the previous simulation, from the node equation of the small signal equivalent circuit, we manage to simplify the Hara active inductor circuit. Then, we input the values and simulate the result of the Bode plot. We also managed to calculate the inductance, L of the Hara active inductance circuit. However the drain current I_d from the simulation is in 10^{-12} order, which seems very small.

In this paper, we reconfirm the characteristic of nMOS by plotting the the I_d to V_{ds} and V_{gs}. Then, we recalculate the R_s and L from previously derived admittance of Hara small signal equivalent circuit. Next, by using the equation and the simulation result, we recalculate the inductance L. Lastly we compare the energy dissipation of 2PASCL inverter using W/L of $0.6\mu m/\ 0.18\mu m$ to the $1.92\mu m/\ 0.18\mu m$.

2 nMOS characteristic simulation

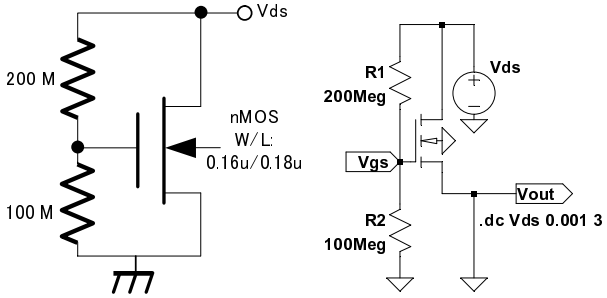

Fig. 1 nMOS evaluation circuit and its SPICE diagram

From this graph, by taking V_{ds} at 1.2V,

$$\begin{aligned} V_{gs} &= \frac{V_{ds}}{R_1 + R_2} R_2 \qquad (1) \\ &= \frac{1.2}{300 \times 10^6} \cdot 100 \times 10^6 \\ &= 0.4\ V, \end{aligned}$$

The value of V_{gs} is as shows in Fig. 7. From Fig. 7 and Fig. 3, the threshold voltage is about 0.5 V.

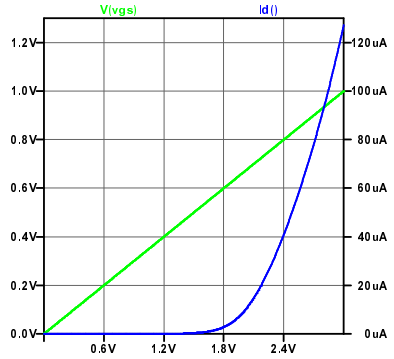

Fig. 2 nMOS evaluation circuit: I_d to V_{ds} and V_{gs} characteristic.

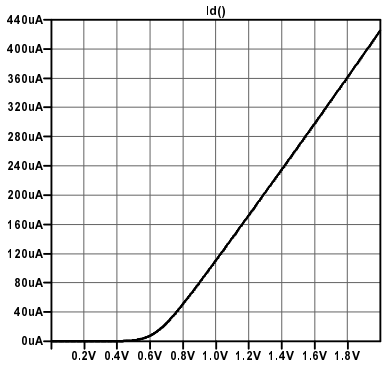

Fig. 3 Drain current I_d vs. V_{gs}.V_{gs} ranging from 0–2 V

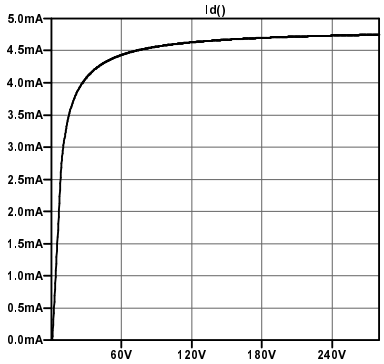

Fig. 4 Drain current I_d vs. V_{gs}.V_{gs} ranging from 0–300 V.

3 R_s and L calculation

Figures 5 and 6 show Hara's active inductor [7] and its small signal model, respectively.

Fig. 6 shows small signal equivalent model. We cal-

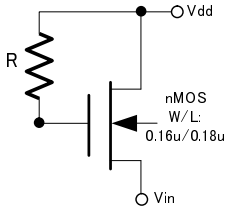

Fig. 5 Hara's active inductor.

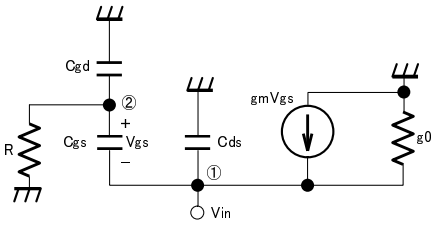

Fig. 6 Small signal equivalent circuit

culate the admittance of this circuit. By using node equation at ① and ②, equations (2) and (3) are derived. Here, since $g_m \gg g_o$ and $C_{gs} \gg C_{gd}$, g_o and C_{gd} are ignored to simplify the results.

$$I_{in} + g_m V_{gs} - j\omega C_{ds} V_{in} + j\omega C_{gs} V_{gs} = 0, \quad (2)$$

$$-j\omega C_{gs} V_{gs} - \frac{1}{R}(V_{in} + V_{gs}) = 0, \quad (3)$$

tranforming above equation (2) and (3), we will get

$$I_{in} - j\omega C_{ds} V_{in} + (j\omega C_{gs} + g_m) V_{gs} = 0, \quad (4)$$

$$V_{gs} = \frac{1}{-Rj\omega C_{gs} - 1} V_{in} = 0, \quad (5)$$

by inserting eq. 5 into 4,

$$I_{in} = \left(j\omega C_{ds} + \frac{g_m}{j\omega C_{gs} R + 1} + \frac{j\omega C_{gs}}{Rj\omega C_{gs} + 1} \right) V_{in}, \quad (6)$$

and it could be rewritten as

$$I_{in} = \left(j\omega C_{ds} + \frac{1}{j\omega \frac{C_{gs} R}{g_m} + \frac{1}{g_m}} + \frac{1}{R + \frac{1}{j\omega C_{gs}}} \right) V_{in}, \quad (7)$$

from eq. 6 by ingnoring C_{ds}, the equation could be rearrage as

$$Y_{in} = \frac{g_m + j\omega C_{gs}}{j\omega C_{gs} R + 1}, \quad (8)$$

therefore,

$$\begin{aligned} Z_{in} &= \frac{j\omega C_{gs} R + 1}{g_m + j\omega C_{gs}}, \quad (9) \\ &= \frac{(j\omega C_{gs} R + 1)(g_m - j\omega C_{gs})}{g_m^2 + (\omega C_{gs})^2}, \\ &= \frac{g_m + (\omega C_{gs} R)^2 + j\omega C_{gs}(g_m R - 1)}{g_m^2 + (\omega C_{gs})^2}, \\ &= \frac{g_m + (\omega C_{gs})^2 R}{g_m^2 + (\omega C_{gs})^2} + j\omega \cdot \frac{C_{gs}(g_m R - 1)}{g_m^2 + (\omega C_{gs})^2}. \end{aligned}$$

Therefore,

$$\begin{aligned} R_s &= \frac{g_m + (\omega C_{gs})^2 R}{g_m^2 + (\omega C_{gs})^2}, \\ L_s &= \frac{C_{gs}(g_m R - 1)}{g_m^2 + (\omega C_{gs})^2}, \end{aligned} \quad (10)$$

as $\omega \to 0$,

$$\begin{aligned} R_s &= \frac{1}{g_m}, \\ L_s &= \frac{C_{gs}(g_m R - 1)}{g_m^2} \cong \frac{C_g s R}{g_m}, \end{aligned} \quad (11)$$

3.1 Calculation of inductance, L

The overlapped gate-source capacitance,

$$\begin{aligned} C_{gs} &= CGSO \cdot W \ (Farads), \quad (12) \\ &= 3.81 \times 10^{-10} \cdot 200 \times 10^{-6}, \\ &= 7.62 \times 10^{-14} \ [F]. \end{aligned}$$

the oxide capacitance, C'_{ox} is

$$\begin{aligned} C'_{ox} &= \frac{\varepsilon_{ox}}{T_{ox}}, \quad (13) \\ &= \frac{3.97 \cdot 8.85[aF/\mu m]}{4.22 \times 10^{-3}[\mu m]}, \\ &= 8.32 \times 10^3 \ [aF/\mu m^2]. \end{aligned}$$

as the hole mobility in nMOS, $\mu_n = 527.2 \ [cm^2/Vs]$, the transconductance parameter, KP is

$$\begin{aligned} KP &= \mu_n C'_{ox} \quad (14) \\ &= 527.2[cm^2/Vs] \cdot 832 \times 10^3 [aF/\mu m^2] \\ &= 43.8 \times 10^{-5} \ [A/v^2]. \end{aligned}$$

From Fig. 8, I_d=1.35×10^{-5}. Thus, the tranconductance, g_m,

$$g_m = \sqrt{2\beta I_D} \quad (15)$$

$$\beta = KP \cdot \frac{W}{L} \quad (16)$$

$$\begin{aligned} g_m &= \sqrt{2 \cdot 43.8 \times 10^{-5} \cdot \frac{200.0}{0.18} \cdot 1.35 \times 10^{-5}}, \\ &= 3.63. \ [mS] \end{aligned}$$

from equation. 11, we calculate L as follows,

$$\begin{aligned} L &= \frac{7.62 \times 10^{-14} \cdot 200 \times 10^{6}}{3.63 \times 10^{-3}}, \\ &= 4.20.\mu H \end{aligned}$$

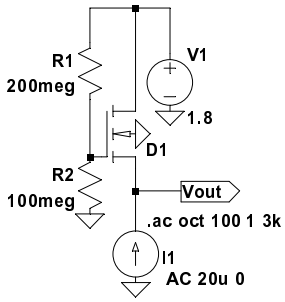

Fig. 7 nMOS evaluation circuit: I_d to V_{ds} and V_{gs} characteristic.

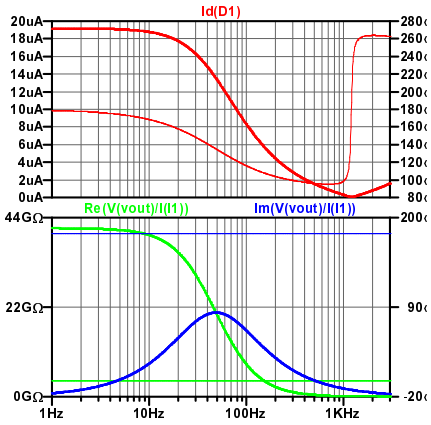

Fig. 8 nMOS evaluation circuit: I_d to V_{ds} and V_{gs} characteristic.

3.2 new W for nMOS

At 100 MHz, the energy dissipation for 2PASCL inverter are as follows

Table 1 Energy dissipation comparison at different channel width

W/L	energy dissipation [μW]
0.6/0.18	0.443
1.92/0.18	0.308

4 Conclusion

We have confirmed the nMOS evaluation simulation by getting the correct I_d to V_ds and V_ds graph. Then the calculation for R_s and L_s equation for Hara active inductor is also carried out. The calculation of L shows in the result. Then, the simulation on inductance is done. The new 1.92 channel width shows lower energy dissipation at transition frequency of 100 MHz.

References

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