Voltage driver and clock circuit for 2PASCL

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Abstract

The paper presents a split-level sinusoidal power supply clock circuit for Two-Phase Adiabatic Static CMOS Logic circuit (2PASCL). We investigate the most suitable scheme which provide the highest efficiency for energy recovery power supply clocks using SPICE simulation.

1 Introduction

In this paper, we design the simplest LC to generate a complementary split level sinusoidal waveforms to drive the proposed 2PASCL logic circuit.

2 Simulation and results

As shown in Fig. 1, a circuit consist of DC power voltage, inductor L, capacitor C and nMOS transistor of W/L of $12.4\mu/0.18\mu$ is used to generate a complementary split level sinusoidal driving voltage and clock for 2PASCL circuit. One is in phase and one is inverted. To generate a $V_{dd}/2$ higher of $\overline{\phi}$, as demonstrated in Fig. 2, $V_{dd}/2$ is added in series to the output.

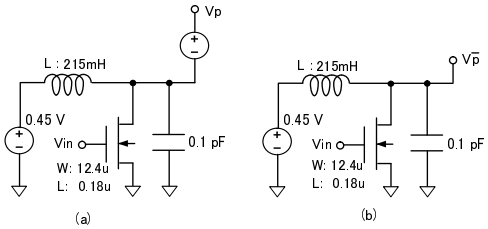

Fig. 1 (a) Circuit to generate ϕ (b) Circuit to generate $\overline{\phi}$.

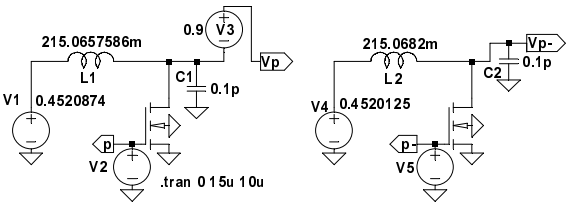

Fig. 2 SPICE diagram of the clock voltage driver with values of each component is detailed.

The result of the simulation is as plotted in Fig. 3

For the next simulation, the above driving voltage is applied to 2PASCL inverter as shown in the diagram of Fig. 4

The simulation result is demonstrated in the graphs of Fig. 6. As the designed clock circuit frequency is 1 MHz, the maximum transition frequency for the logic is 250 kHz. At this frequency, the power consumption is 18.6 nW. Compared to the default power clock used in the SPICE simulation, at 250 kHz it is only 2.62 nW. Therefore the default clock is 85.9% lower than the designed LC clocked shown in 1.

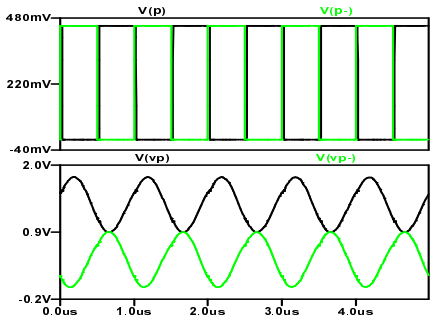

Fig. 3 Simulation result of the proposed voltage power clock circuit. f=250 kHz

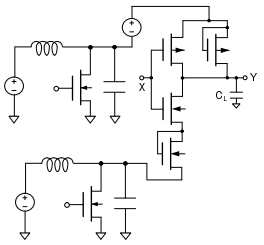

Fig. 4 Schematic of the 2PASCL connected with the driving power clock circuit.

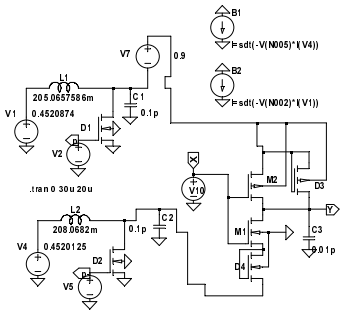

Fig. 5 SPICE diagram of the application.

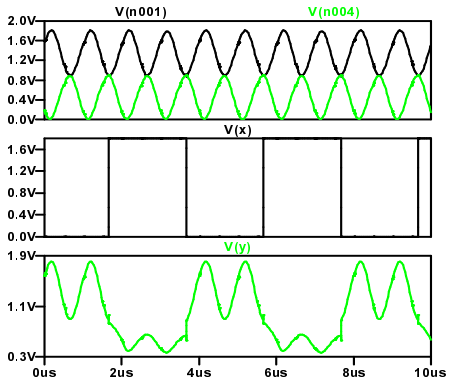

Fig. 6 Simulation result of the 2PASCL inverter using the driving voltage clock circuit.

3 Conclusion

We have designed and simulated the complementary split level sinusoidal waveforms to drive and used as clock for 2PASCL. It is using the LC circuit with $V_{dd}/2$ power voltage connected in series to create the ϕ which is $V_{dd}/2$ V higher than $\overline{\phi}$. However, the result of the energy dissipation shows that it is 85.9 % higher compared when using the default clock in SPICE simulation. The clock needs to be redesigned with appropriate parameters in order to reduce the energy consumption in the 2PASCL logic circuits.