2PASCL - Power clocks comparison and unsymmetrical evaluation

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Abstract

The paper demonstrates SPICE simulations on different power clocks frequency of 100 MHz transition frequency of 2PASCL and 2PADCL. Power dissipation of symmetrical compared to unsymmetrical split-level sinusoidal power clocks is also carried out. From the simulation results, we find that 2PASCL show the lowest power dissipation at symmetrical power clocks with 2 and 4 times clock frequencies compared to transition frequency.

1 Introduction

We have seen a significant power dissipation in 2PASCL NOT gates. However, we are still yet to confirm on which power clock frequency or whether symmetrical or unsymmetrical power clocks contribute to lower power dissipation.

In this study, we simulate several power clock frequencies and a few combination of unsymmetrical power clocks and see the power dissipation results.

2 Power supply clock frequency comparisons

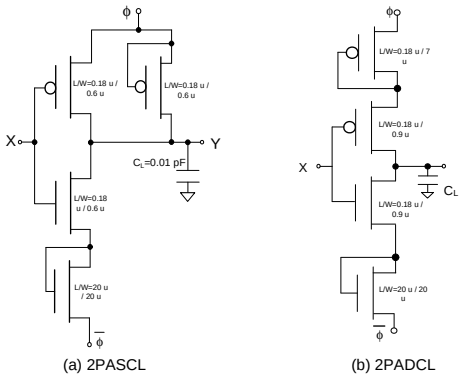

Fig. 1 Circuit diagram of 2PASCL and 2PADCL.

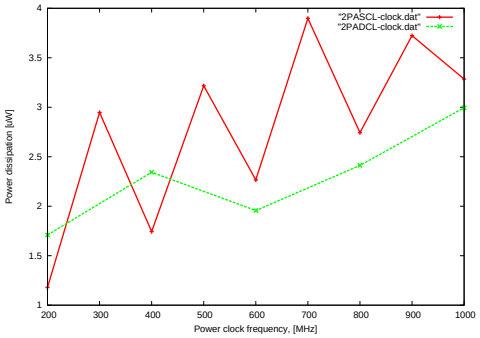

Fig. 2 Power dissipation when power supply clocks are set to be 2x,3x,4x,5x,6x,7x,8x,9x,10x for 2PASCL and 2x,4x,6x,8x,10x for 2PADCL. Transition frequencies are 100 MHz for both circuits.

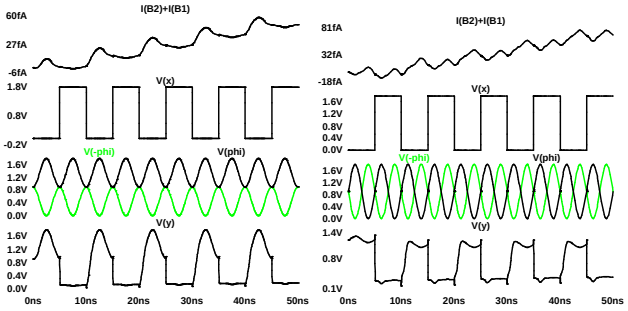

Fig. 3 Output waveforms of 2PASCL (left) and 2PADCL (right) when clock frequency is 2x of transition frequency.

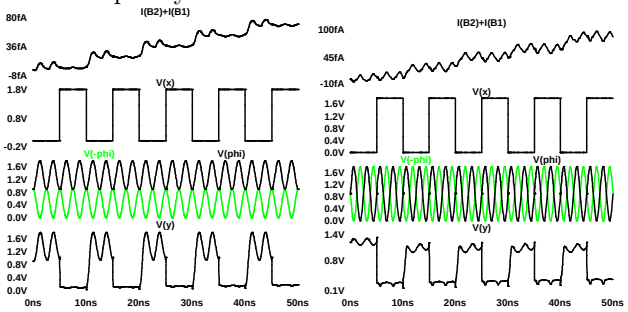

Fig. 4 Output waveforms of 2PASCL (left) and 2PADCL (right) when clock frequency is 4x of transition frequency.

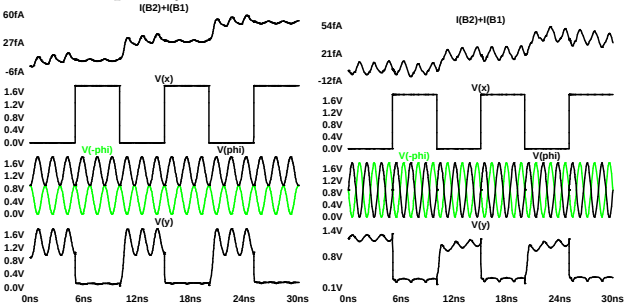

Fig. 5 Output waveforms of 2PASCL (left) and 2PADCL (right) when clock frequency is 6x of transition frequency.

3 Unsymmetrical clocks supply for 2PASCL

Next, we evaluate a few unsymmetrical ratio and compared the power dissipation. The results are shown in Table 1

4 Inverter chain

5 Conclusion

From the results, 2PASCL shows the lowest energy dissipation at symmetrical split level sinusoidal and at the clock frequency when it is 2X the transition fre-

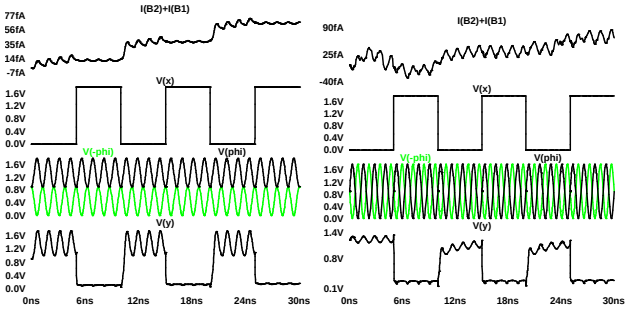

Fig. 6 Output waveforms of 2PASCL (left) and 2PADCL (right) when clock frequency is 8x of transition frequency.

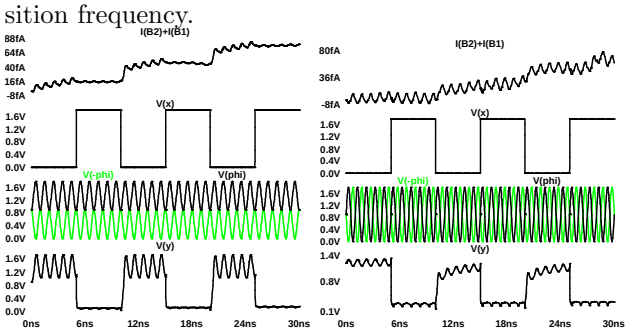

Fig. 7 Output waveforms of 2PASCL (left) and 2PADCL (right) when clock frequency is 10x of transition frequency.

Table 1 Power dissipation for different unsymmetrical power clocks of 100 MHz 2PASCL

ϕ	$\overline{\phi}$	Power dissipation [uW]
0.9	0.9	1.18
1.1	0.7	1.64
1.3	0.5	2.20
1.5	0.3	2.63
1.7	0.1	3.36
0.5	1.3	1.14

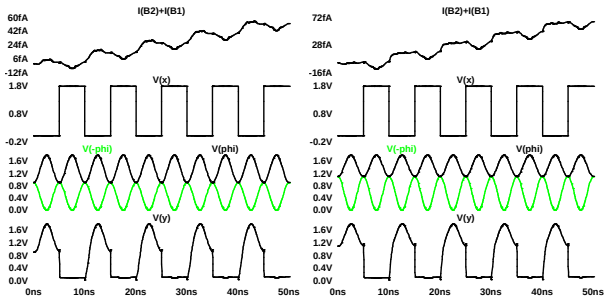

Fig. 8 Symmetrical clocks; phi(-)=0.9 V and phi=0.9 V (left) and unsymmetrical clocks; phi(-)=1.1 V and phi=0.7 V (right).

quency. For 2PASCL 8-inverter chain, it also shows 37% lower than CMOS 8-inverter chain.

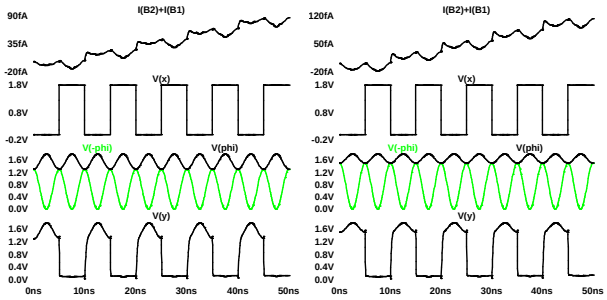

Fig. 9 phi(-)=1.3 V and phi=0.5 V (left) and phi(-)=1.5 V and phi=0.3V (right).

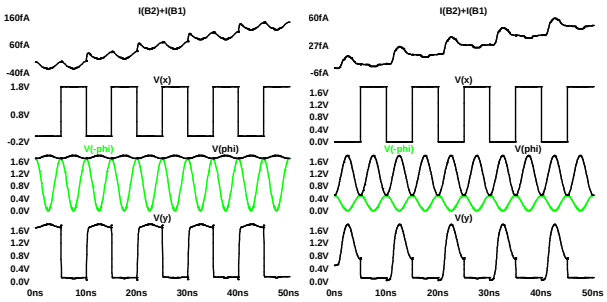

Fig. 10 phi(-)=1.7 V and phi=0.1V (left) and phi(-)=0.5 V and phi=1.3 V.

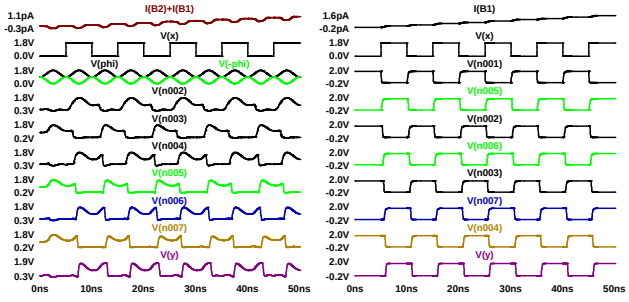

Fig. 11 Output waveforms of 2PASCL 8-inverter chain. At 100 MHz transition frequency, the power dissipation is 221 fJ (left) and Output waveforms of CMOS 8-inverter chain. At 100 MHz transition frequency, the power dissipation is 350 fJ (right).