Low-Power 4×4-Bit Array Two-Phase Clocked Adiabatic Static CMOS Logic Multiplier

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Abstract— This paper presents the simulation results of a 4×4-bit array 2PASCL multiplier and its layout design using 1.2 μm standard CMOS technology. From the SPICE simulation, at transition frequencies of 1 to 12 MHz, 4×4-bit array 2PASCL multiplier shows a maximum of 57% reduction in power dissipation to that of a static CMOS. Observations on the current that flows through the transistors in 2PASCL and CMOS are also presented. From the simulation results, 2PASCL technology can be advantageously applied to low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors.

I. INTRODUCTION

In recent years, various energy recovery circuits with adiabatic circuitary for ultra-low power implementation have been presented [1]–[15]. Adiabatic charging [1] is a principle where all charge transfer is to occur without generating heat. The energy advantage can be understood by assuming a constant current source that delivers the charge $C_L V_{dd}^2$ over a time period T. The dissipation through the channel resistance R is then $E_{diss} = (\frac{RC_L}{T})C_L V_{dd}^2$ [2]. Theoretically, it is possible to reduce the dissipation to an arbitrary degree by increasing the switching time to ever-larger values. Conventional adiabatic logic circuits [1]–[10] that have been proposed shows a much less power dissipation compared with static CMOS circuit. For instance, at 10 MHz clock input, efficient charge recovery logic (ECRL) [10] dissipates only 16% of the energy of static CMOS logic in a chain inverter application. However, most of these circuits require a multiphase power clocks. Several problems, such as a complicated clock design and an increase of energy dissipation due to the power clocks occur. Furthermore, for a single and a two phase clock circuits, diode-based families [4]–[9] have several disadvantages such as output amplitude degradation and the energy dissipation across the diodes in the charging path [16].

At the earlier stage of the 2PASCL [17], we have designed, simulated, and compared the power consumption of 2PASCL NOT, 2NAND, 2XOR, and 2NOR to CMOS topology. We have also discussed the pros and cons of 2PASCL compared to other proposed adiabatic logics that are easily derived from CMOS in [16]. 2PASCL fundamental logics significantly exhibit a lower power dissipation [18]–[19]. In this paper, we simulate a 4×4-bit array 2PASCL multiplier utilizing 1.2 μm standard CMOS technology. Observations on the current that
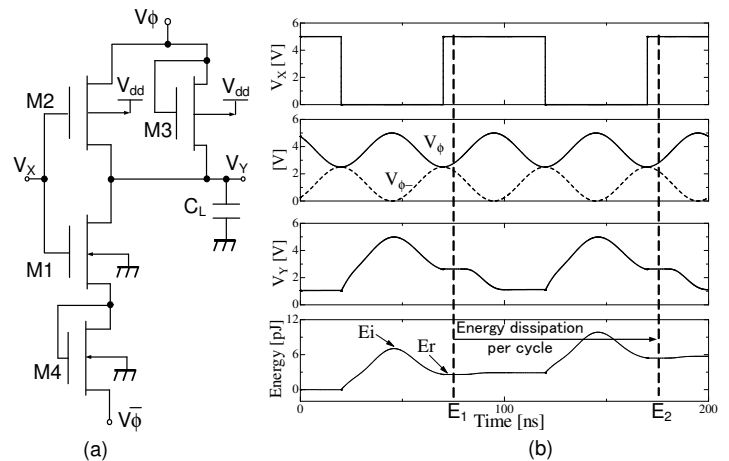

Fig. 1. (a) 2PASCL inverter circuit. (b) Waveforms from the simulation, transition frequency f_T, V_X=10 MHz, $V_\phi = V_{\bar{\phi}}^- = 20$ MHz.

flows in the 2PASCL inverter circuits and the comparison to static CMOS are also carried out. As 2PASCL dissipates less power theoretically and as shown in the simulation results, we also design the layout of the 4×4-bit array 2PASCL multiplier. 2PASCL technology can be advantageously applied to low power digital devices operated at low frequencies, such as radio-frequency identifications (RFIDs), smart cards, and sensors. The summary of the parameters used in 1.2 μm standard CMOS technology are listed in Table I.

The remainder of the paper is organized as follows. Section II describes the structure of 2PASCL inverter and the current flow through the transistors. In Section III, we introduce the 4×4-bit array 2PASCL multiplier. Section IV includes concluding remarks and future work.

II. CMOS CIRCUITS VIS-A-VIS 2PASCL

Figure 1 shows the 2PASCL inverter circuit and the waveforms from the simulation results at 50 MHz transition frequency. 2PASCL has been powered by the split-level sinusoidal power supply clocks [17]–[19]. To generate this, we have presented the proposed circuit in [16]. For the modeling of MOSFETs in both 2PASCL and CMOS, an ideal switch in series is included with a resistor R in order to represent the sum of the effective channel resistance of the switch and
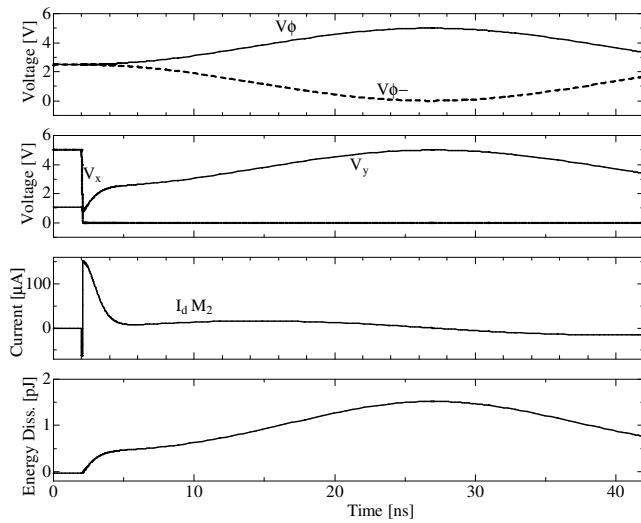
Fig. 2.   Simulation results of current and energy dissipation of 2PASCL during pull-up networks.
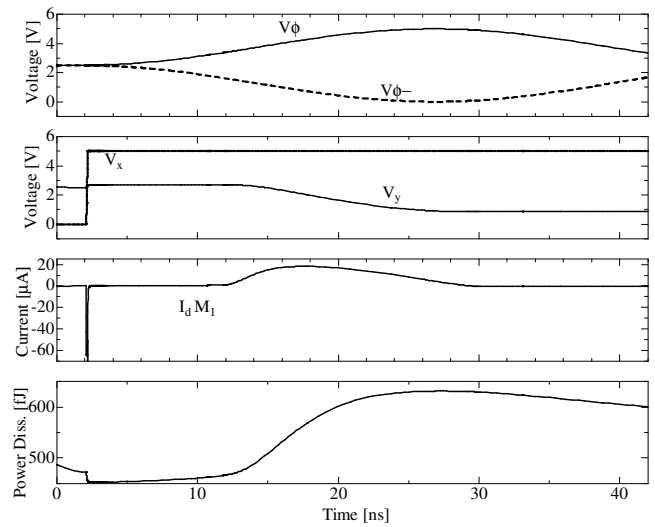

Fig. 4.   Simulation results of current and energy dissipation of 2PASCL during pull-down networks.
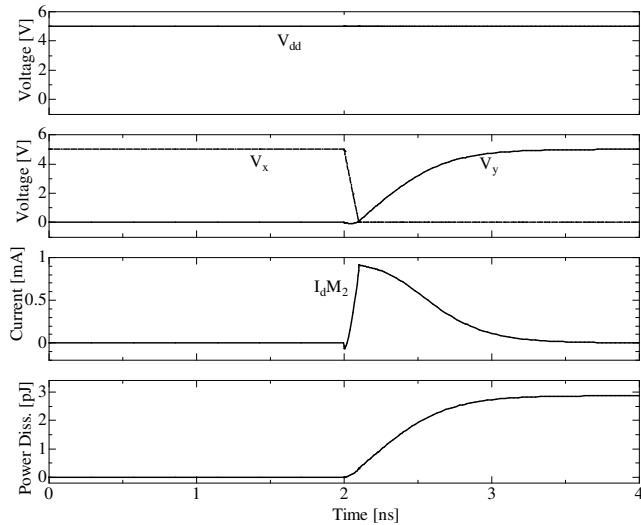

Fig. 3.   Simulation results of current and energy dissipation of CMOS during pull-up networks.
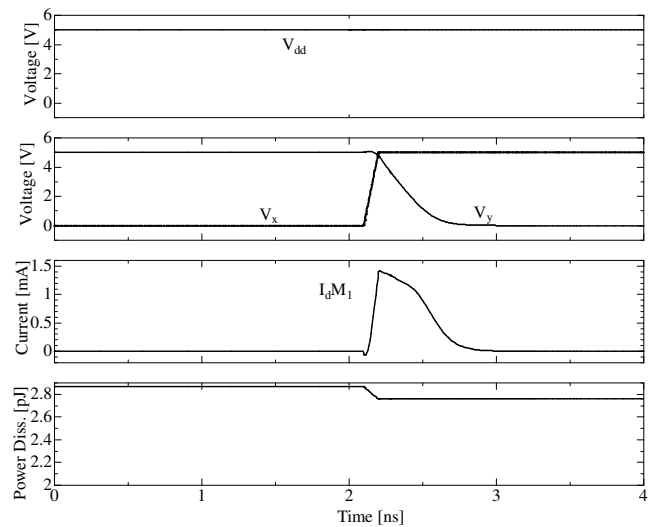

Fig. 5.   Simulation results of current and energy dissipation of CMOS during pull-down networks.

the interconnect resistance. In CMOS, when the logic level in the system is "1," there is a sudden flow of current through R [16]. As the power dissipation is $p(t) = Ri^2$ and the current, $i = C_L \frac{dv}{dt}$, the amount of flowing current can be minimized by reducing the load capacitance and/or the changing rate of supply voltage from 0 to V_{dd}.

In Figs. 2–5, we demonstrate the simulation results of the power clocks and V_{dd} on the top graph, input V_X, 10 MHz and output signal V_Y on the second graph, the drain current I_d on the third graph, and the power dissipation on the fourth graph.

Figure 2 describes the conditions during pull-up networks of 2PASCL inverter. When V_X changes from HI to LO, 144

μA of I_d flows for 2.5 ns. Then from 2.5 to 25 ns, the circuit is operating according to adiabatic manner, when current is seen to be constant at 15 μA. In Fig. 3, as a comparison, we include CMOS inverter simulation results during pull-up networks. As shown in the current flow graph, after the input signal changes from HI to LO, 912 nA of current flows through the resistive elements of the pMOS. This non-adiabatic charging takes about 1.5 ns before resting at 0 V. On the fourth graph of energy dissipation, the dissipated energy of CMOS is 2.5 pJ which is 66% more than 2PASCL. This is the value prior including the total energy dissipation of 2PASCL which has the recovery energy shown in Fig. 2, from 30 to 42 ns.

Figure 4 demonstrates the 2PASCL inverter during pull-

TABLE I

PARAMETERS USED IN THE SIMULATION

	1.2 μm tech.
W/L	5.0 μ/1.2 μ
V_ϕ, $V_{\bar\phi}$	2.5 V, 2.5 V
C_L	0.1 pF
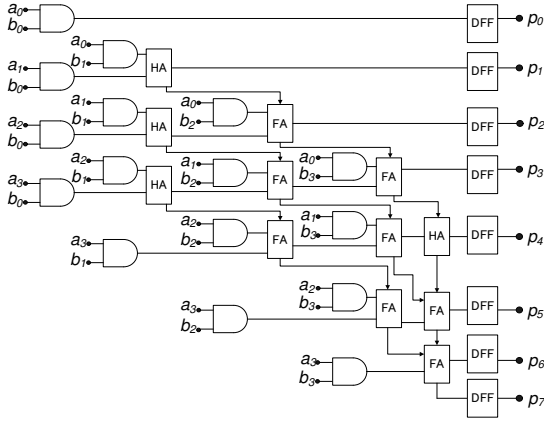
Fig. 6.   Block diagram of 4×4-bit array 2PASCL multiplier with D-flipflop at the outputs.

Fig. 7.   Simulation result 4×4-bit array 2PASCL multiplier with D-Flip Flop using 1.2 μm CMOS technology with transition frequency f_T is 10 MHz.

down networks. After input signal changes from LO to HI, nearly 80 μA flows from the transistor to the output node Y, which we think is a short-circuit current as the rise and fall time of the input signal is 0.1 ns. Since the short-circuit current occurs in CMOS inverter as well, we will identify this matter in future. From 12 to 30 ns, we also observe that 2PASCL circuit is operating in adiabatic mode. The current pass through the nMOS transistor M1 is about 15 μA. The energy dissipation from the fourth graph also show that only 0.63 pJ is dissipated before the recovery mode starts from 30 ns to 42 ns. In Fig. 5, we describe the current flow in nMOS of CMOS during pull-down networks. Almost the same as pull-up, 1.5 mA of current flows to the nMOS transistor during the logic transition. Due to the short-circuit current at 2.1 ns, the energy dissipation reduced for about 0.2 pJ. However the energy dissipation of 2.8 pJ in CMOS is still four times larger compared with 2PASCL.

From this current and energy evaluation, a significant lower current flowing in 2PASCL than CMOS is observed, consequently reducing the energy dissipation during transition by utilizing adiabatic principle.

III. 4×4-BIT ARRAY 2PASCL MULTIPLIER

Evaluation on the four XOR candidates have been carried out in [20]. We have selected the XOR that provide the least number of transistors, low power dissipation and least glitches in the output waveforms. Figure 6 shows the block diagram of 4×4-bit array multiplier which consists of sixteen ANDs, six full adders, four half adders logics, and eight D-flip flop at all outputs (p_0 to p_7). In Fig. 7, we demonstrate the simulation results of 4×4-bit array 2PASCL multiplier utilizing 1.2 μm
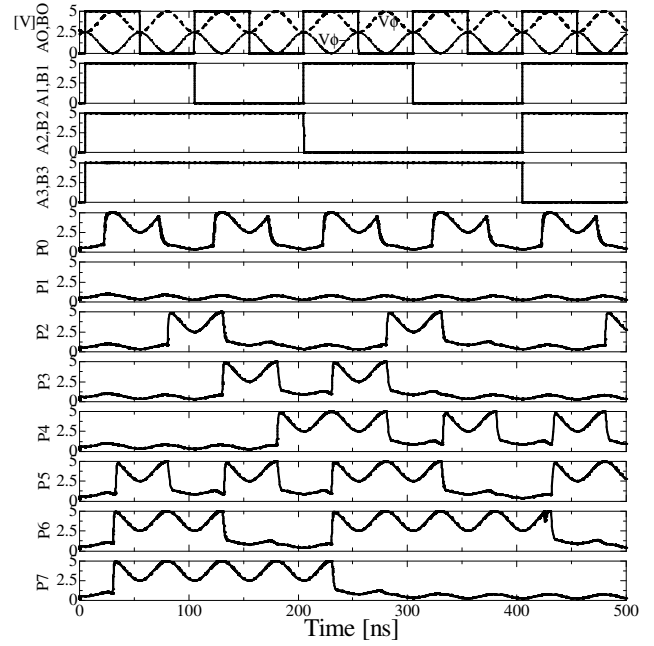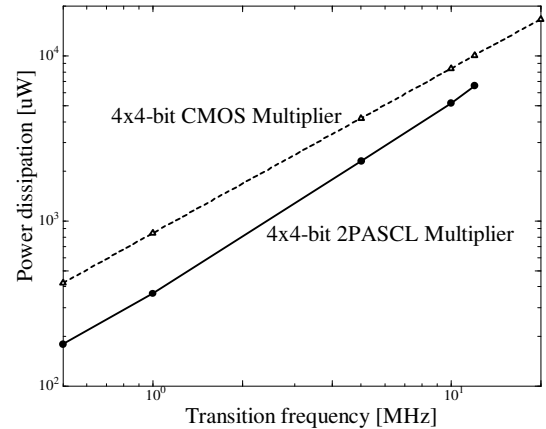

Fig. 8.   Power dissipation comparison of 4×4-bit array 2PASCL multiplier and 4×4-bit array CMOS multiplier using 1.2 μm CMOS technology.

CMOS technology. In this simulation, we also add 2PASCL D-flipflops [17] to capture all the 8-bit signals at the moment the clock is in HI state. As shown in Fig. 1 (b), in energy-recovery circuits, from the energy conservation law, energy dissipated is equal to the total of energy injected to the circuit, E_i and the energy received back from the circuit capacitance, E_r. In the simulation, the power dissipated is calculated by integrating the product of voltage and current divided by the period of the primary input signal, T as follows:

$$P = \frac{1}{T} \int_0^T \left(\sum_{i=1}^n (V_{pi} I_{pi}) \right) dt, \qquad (1)$$
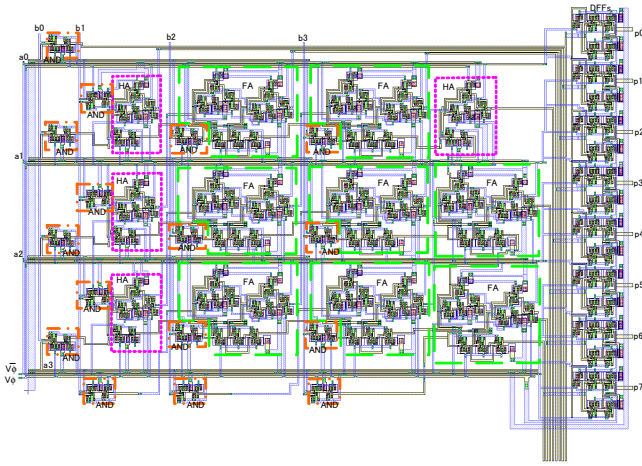
Fig. 9. The layout of 4×4-bit array 2PASCL multiplier using 1.2 μm CMOS technology.

TABLE II
CHIP SUMMARY.

Technology	1.2 μm CMOS 2-metal, 2-poly
Power Voltage	5.0 V
Core Size	1354 (W) × 997 (H) μm^2
No. of transistors	992
Dynamic Operating Frequency	5–50 MHz (from simulation)
Dynamic Power Dissipation	4 mW@ 10 MHz (from simulation)

where V_p, the power supply voltage; I_p, the power supply current; and n, is the number of power supplies [8].

Figure 8 shows the power dissipation of 2PASCL multipliers which has up to 57% less than CMOS multipliers. However, from our simulation results, 4×4-bit array 2PASCL multiplier only shows a good logic functionality of up to 12 MHz transition frequency. We observed some signal degradations for transition frequency of more than 12 MHz. This is due to the charging time T which is much slower than conventional CMOS. T is also proportional to RC_L i.e. the longer the path, the larger T is needed. These input frequencies are adequate for the applications mentioned in Section I. From these results, we fabricate a 4×4-bit array 2PASCL multiplier using 1.2 μm CMOS technology. A multiblock layout is shown in Fig. 9. Eight D-Flip flops are connected at each output of p_0 to p_7. The chip summary is listed in Table II.

IV. CONCLUSION

In this paper we have designed and simulated a 4×4-bit array two-phase clocked adiabatic CMOS logic (2PASCL) multiplier circuit using a new 2XOR. The simulation results show that power consumption in the 2PASCL multiplier is considerably less than that in a CMOS. For instance, when the input frequency is simulated from 1 to 100 MHz, the 2PASCL multiplier logic dissipates minimally as only half of the power dissipated by a static CMOS logic circuit. We believe that the proposed adiabatic logic circuit is advantageous for ultra low-energy computing applications. As for our future work, we will further evaluate the short-circuit currents in both 2PASCL and CMOS.

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