PAPER

Low-power Adiabatic Logic Circuit Simulation and Energy Dissipation Comparison

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SUMMARY This paper investigates the design approaches of low-power adiabatic logic gates in terms of energy dissipation associated with the input transition. A computer simulation using LTSpice is carried out on several inverter circuits implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the logic gates. The dissipation characteristics are also compared at the different load capacitance values.

key words: *adiabatic logic*

Presentation content

- 2008/09/26 : Circuit Simulation and Energy dissipation at different C
- 2008/10/03 : Circuit Simulation and Energy dissipation at different C (continue)
- 2008/10/10 : Circuit Simulation with new diagrams
- 2008/10/17 : More Circuit Simulation and Energy Dissipation comparison

1. Introduction

The development of CMOS technology provides high density and high performance to integrated circuits. As the density of an integrated circuit increases, the power consumption increases and its temperature control becomes difficult. Moreover, mobile devices require a high performance, light weight, and long operation time, which are contradictory characteristics. Adiabatic computing is an attractive approach in this viewpoint. In recent years, studies on adiabatic computing have been grown for low power systems and several adiabatic logic families have been proposed.

1.1 Adiabatic Logic Circuit Group

1.1.1 Asymptotically Adiabatic Logic

In [1], asymtotically adiabatic logic comprised of circuits in which dissipation results solely from finite rate of change of driving voltage and can be decreased to any desired level. In [1], it is represented by 2n2p-2n logic, 1n1p logic that is using the split-level driving pulses and split-level charge-recovery logic.

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1.1.2 Quasi-Adiabatic Logic

In [1], quasi-adiabatic logic comprised of circuits which dissipation can be reduced appreciably by lowering the rate of change of driving voltage. It is divided into another 2 groups, which is the static approach and the dynamic approach. The static is represented by 1n-1p and 2n-2n2p quasi-adiabatic logic. While the dynamic approach is represented by Hot-Clock nMOS (HCnMOS) logic, Recovered-Energy logic (REL), Adiabatic Dynamic Logic (ADL), Efficient charge-recovery logic (ECRL), Adiabatic Dynamic CMOS Logic (ADCL) and 2-Phase Adiabatic Dynamic CMOS Logic (2PADCL).

2. Simulation and Results

2.1 Conditions

The paper starts by examining the functional and energy dissipation of a simple logic gate, an inverter. The simulations using LTSpice are carried out for all the circuits reviewed in [1]. Circuits are connected to the pulse driving voltage and input signal according to the layouts. The operation clock frequency is 50 MHz. Length and width of the nMOS and pMOS logic gates used in this simulation are L=0.18 μm, W=0.6 μm. The most suitable load capacitor value for each circuits is examined according to the output voltage waveforms. Circuits diagrams and simulation results in the form of waveforms are represented by Fig. 2 – Fig. 12. The energy dissipation is calculated by integrating the voltage and current product value as follows

$$E = \int_0^{T_s} (\sum_{i=1}^{n} (V_{pi} \times I_{pi}))dt \quad (1)$$

where T_s is the period of the primary input signal, V_p is the power supply voltage, I_p is the power supply current and i is a number of power supply [2].

2.2 Circuits comparison

Table 1 lists the features of all logics in the review for comparison. In this preliminary results, ADL show the

lowest value of energy dissipated per cycle while 2n-2n2p quasi adiabatic show the highest. 8 out of 10 adiatic circuits show a lower energy dissipation compared to conventional static CMOS by reducing from 98% to 17%.

2.3 Energy dissipation at different load capacitance

The simulation result on the energy dissipation at different load capacitance is shown in Fig. 13. As expected, all the circuits, except 2PADCL show an increase of dissipated energy when changing the load capacitor to a higher value.

3. Conclusion

- Analysis of the adiabatic circuits using LTSpice shown that the energy dissipation per cycle can be calculated and therefore is convinience for futher analysis and design. In this simulation result, ADL shows the lowest energy dissipation as an inverter
- Load Capacitance which use as the data holder need to be design precisely considering the time constant that effect the output and also the amount of information to be stored
- Unlike other circuits 2PADCL shows a decrease in energy dissipation when the load capacitance increased. If this is true, this circuit has a higher possibility to be further studied
- REL in MOSFETs circuits are still not operating very well in this simulation. Further corrections need to be carried out.

References

[1] V.I Starosel'skii "Adiabatic Logic Circuits: A Review," *Russian Microelectronics,* 2002, Vol.31, No. 1, pp.37-58
[2] Y. Takahashi, Y. Fukuta, T. Sekine, and M. Yokoyama, "2PADCL : Two Phase drive Adiabatic Dynamic CMOS Logic, " *Proc. IEEE APCCAS,* Dec 2006, pp. 1486-1489

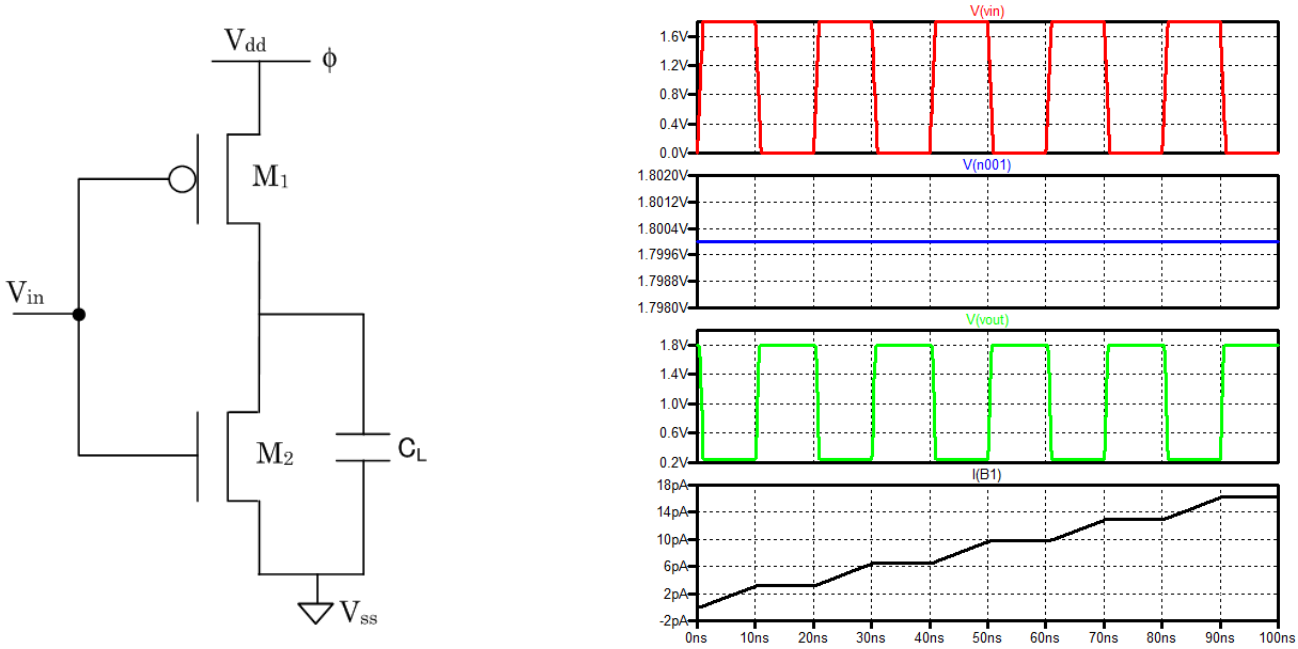

Fig. 1 Conventional CMOS logic inverter circuits diagram and waveforms

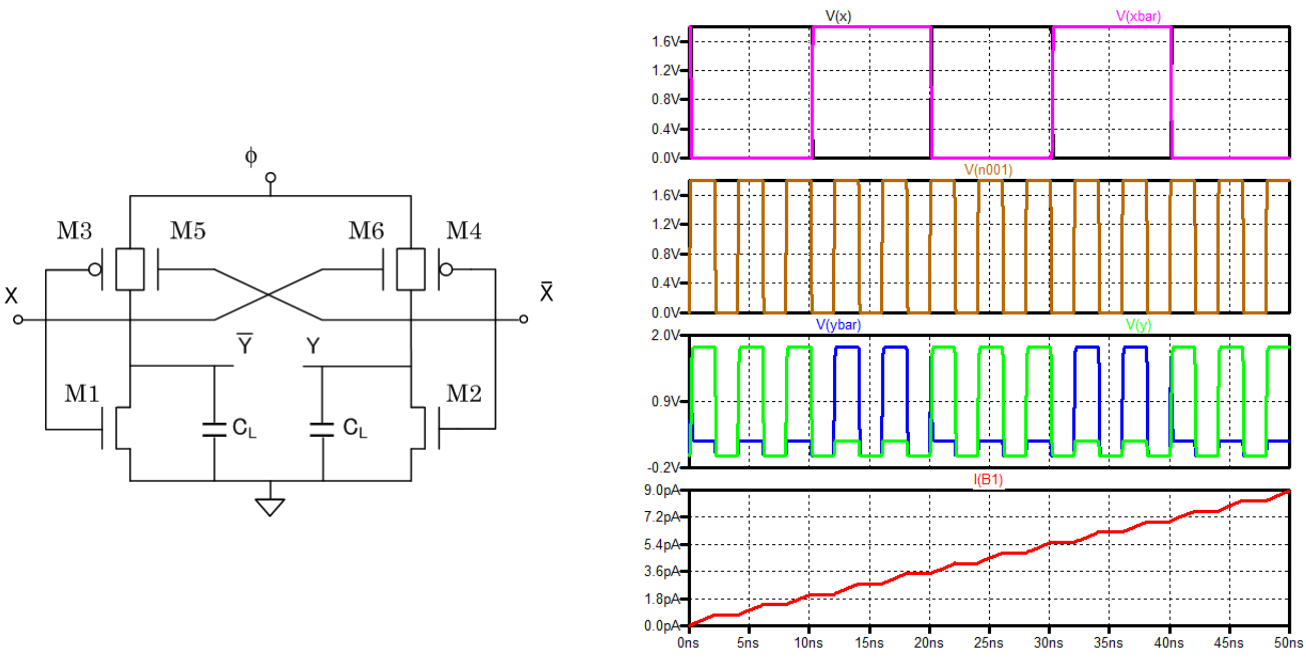

Fig. 2 2n2p-2n adiabatic logic inverter circuits diagram and waveforms

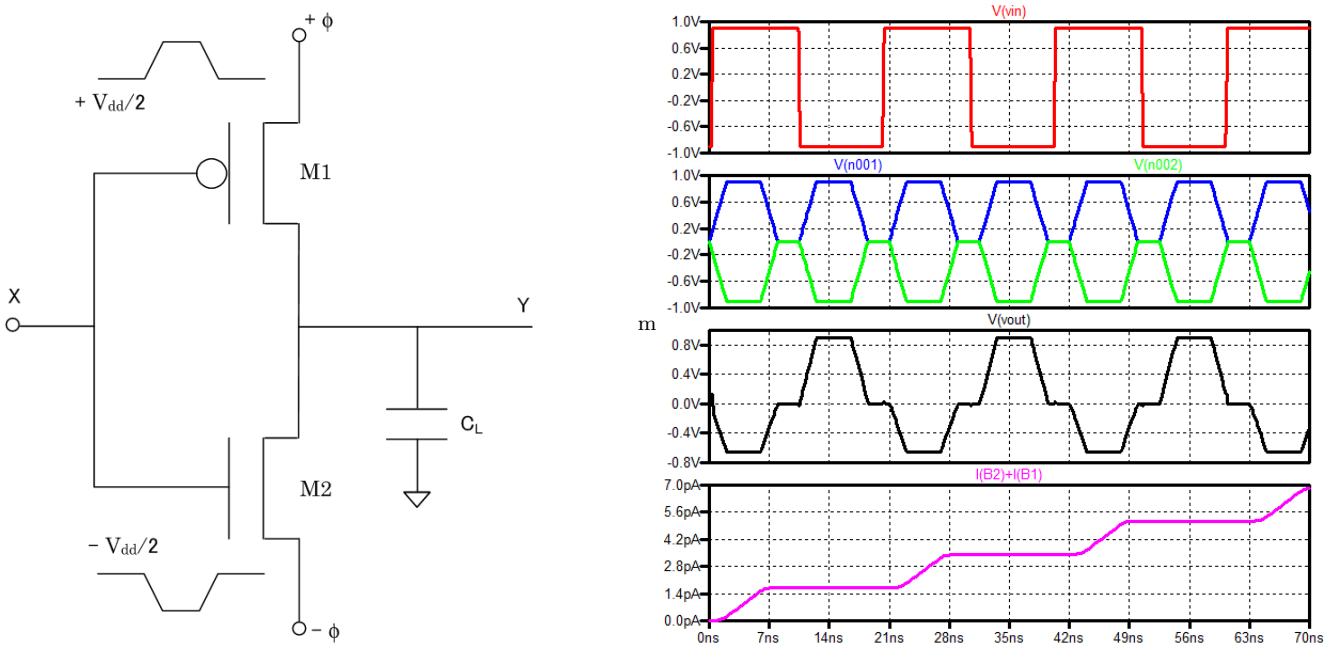

Fig. 3 Split level pulse 1n1p logic inverter circuits diagram and waveforms

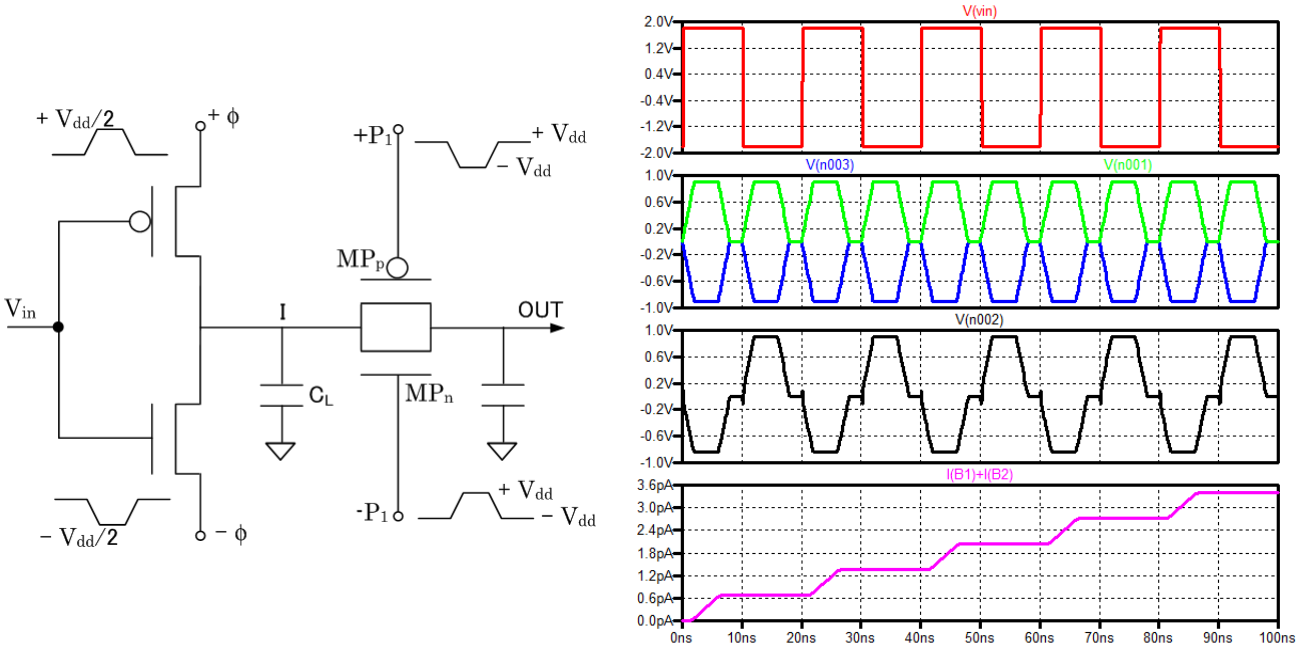

Fig. 4 Split level charge-recovery logic inverter circuits diagram and waveforms

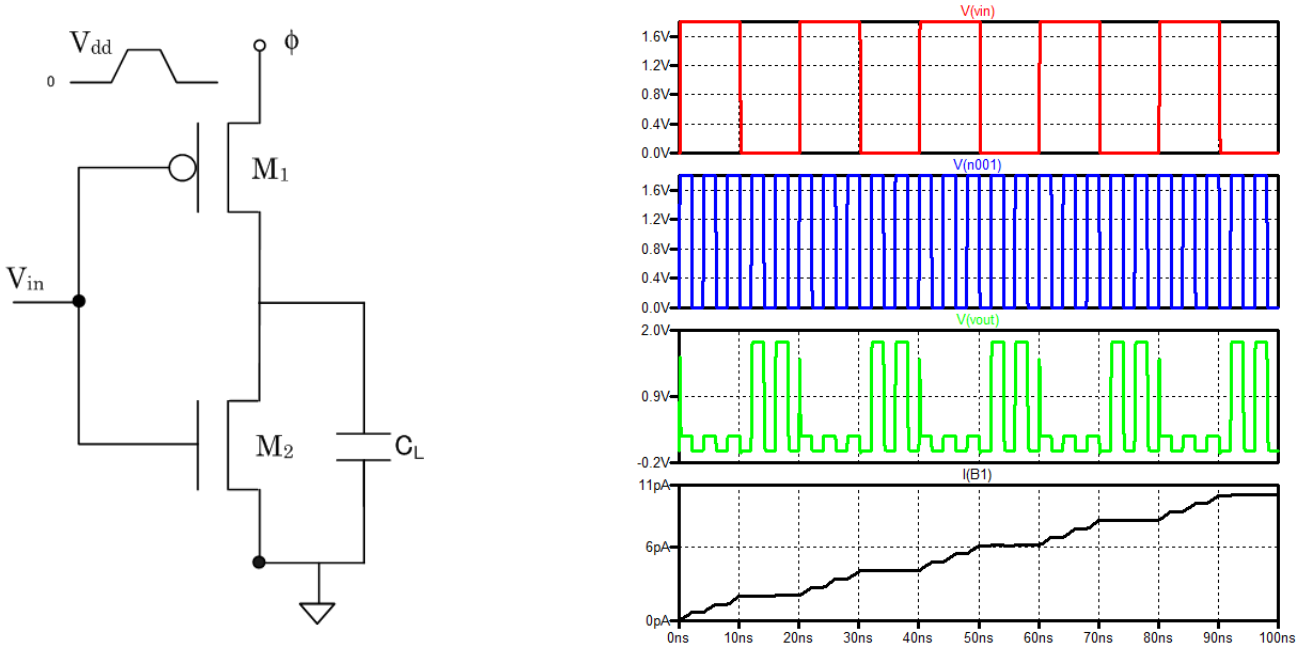

Fig. 5 1n-1p quasi-adiabatic logic inverter circuits diagram and waveforms

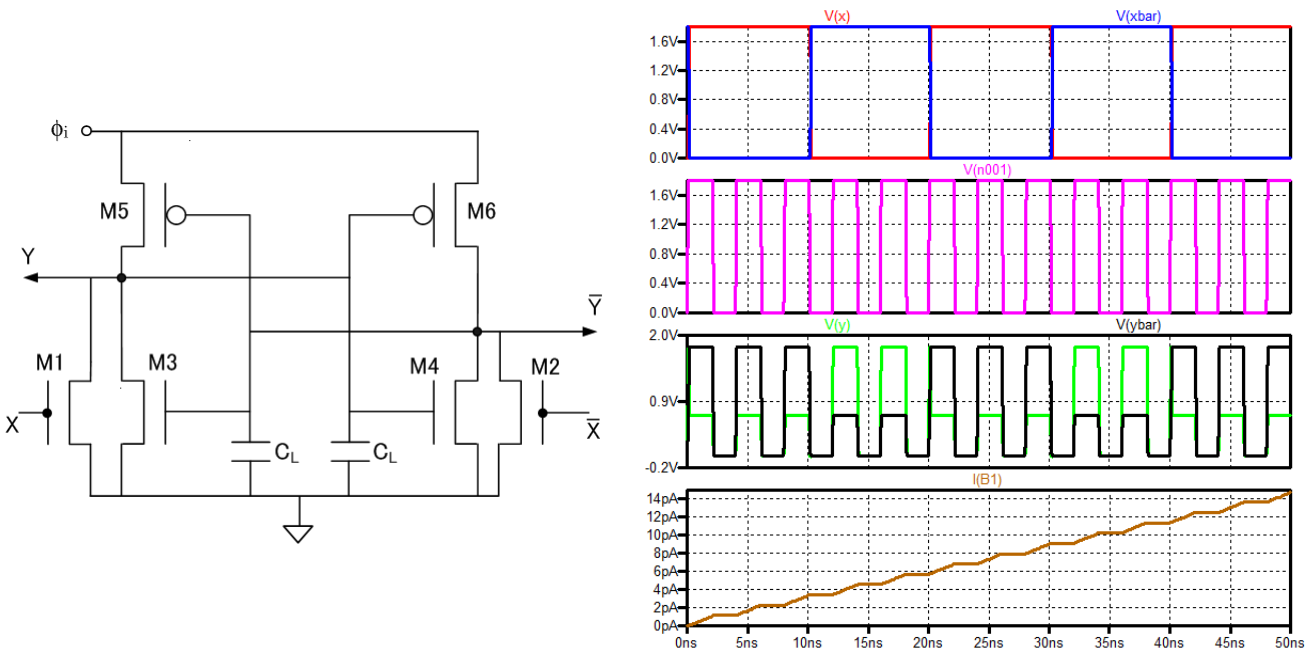

Fig. 6 2n-2n2p quasi-adiabatic logic inverter circuits diagram and waveforms

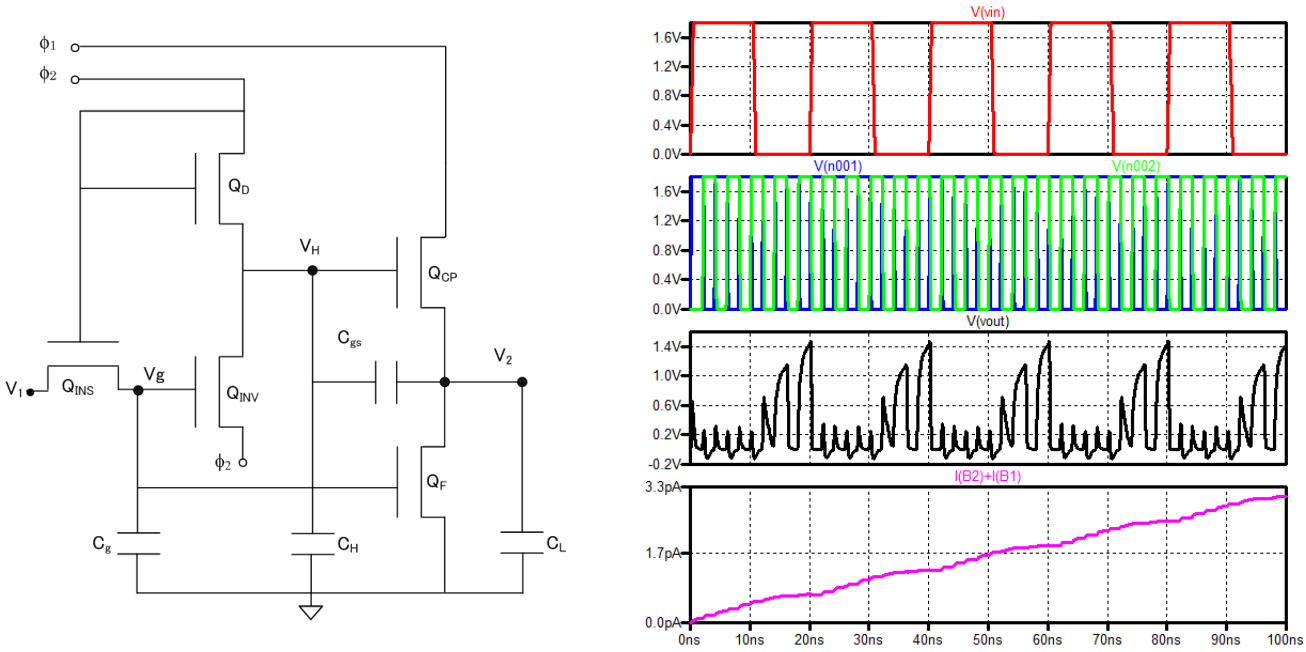

Fig. 7 Hot-clock nMOS logic inverter circuits diagram and waveforms

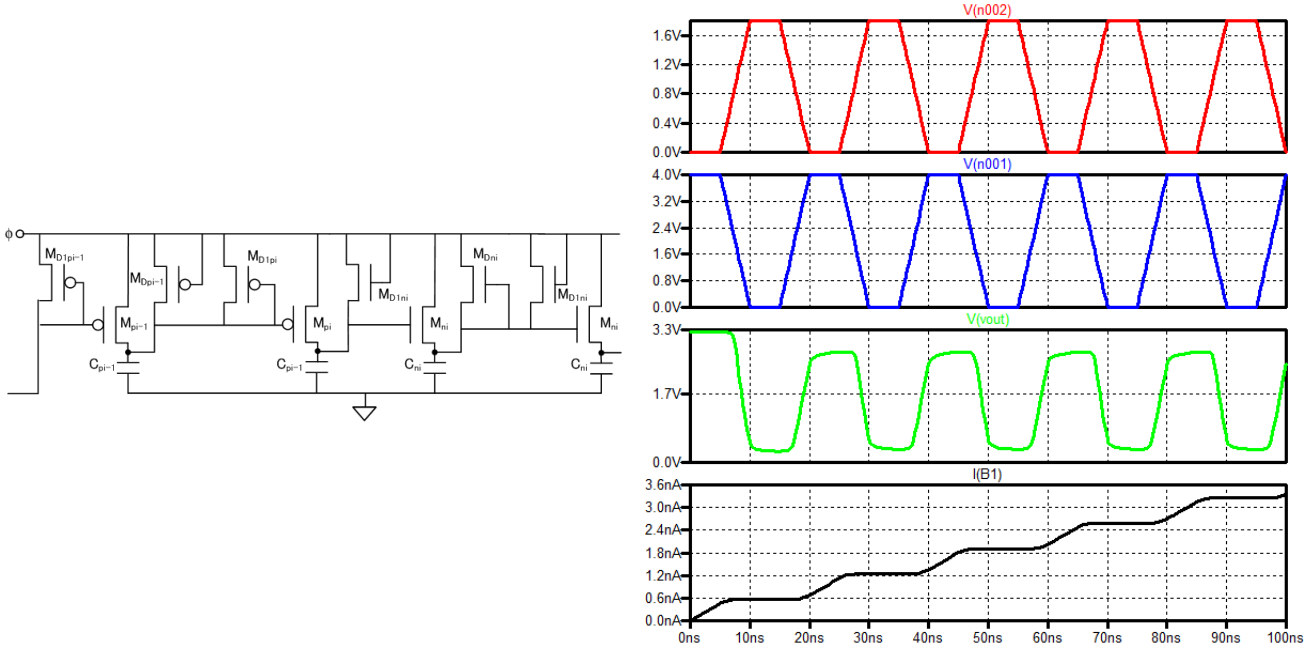

Fig. 8 Recovered-energy logic (REL) in MOSFETs inverter circuits diagram and waveforms

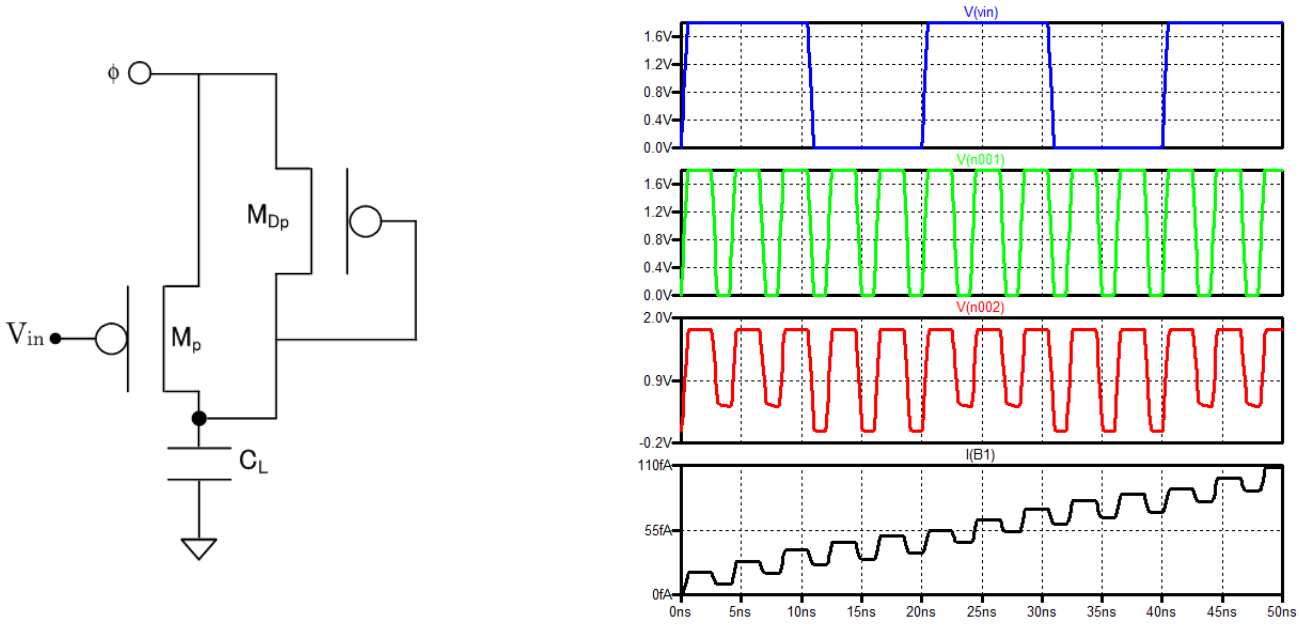

Fig. 9 Adiabatic Dynamic logic (ADL) inverter circuits diagram and waveforms

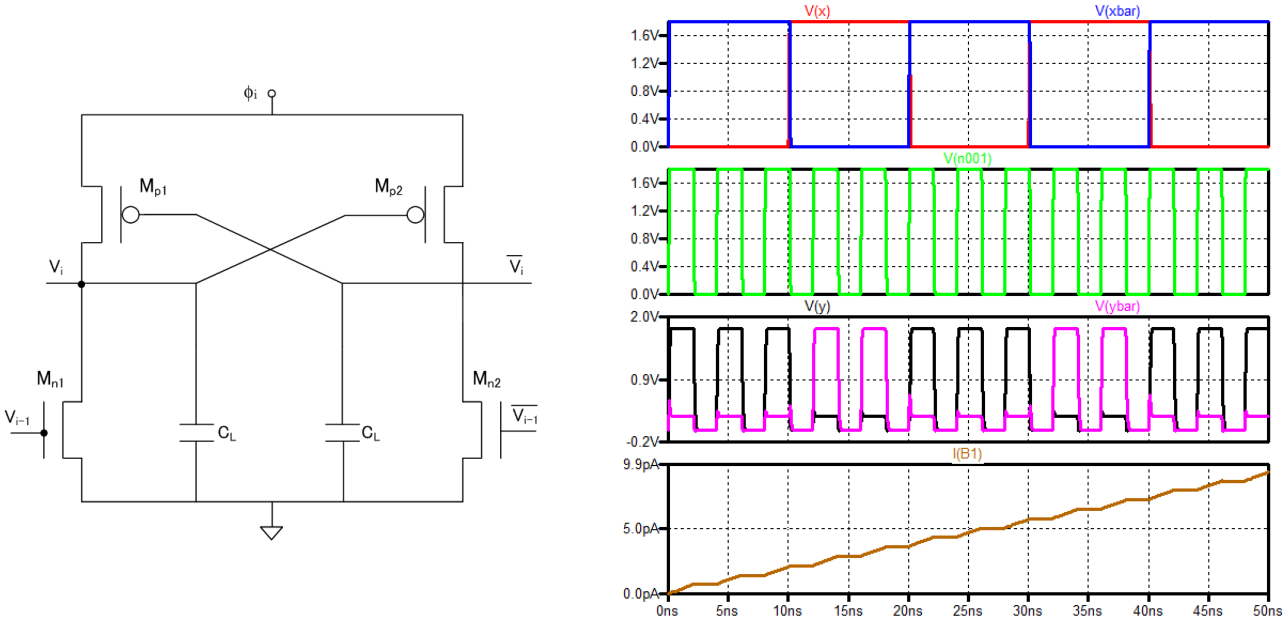

Fig. 10 Efficient charge-recovery logic (ECRL) circuits diagram and waveforms

Table 1 Comparison of Power Dissipation

Adiabatic Logic Circuits	Energy Dissipation (pJ/cycle)	Number of Gates	Driving Pulse
ADL	0.035	4	4
1n-1p Split level charge recovery	0.53	4	1
HCnMOS	0.60	5	2
2PADCL	0.769	4	2
ECRL	1.28	4	1
ADCL	1.13	4	1
1n-1p quasi	2.05	2	1
1n-1p Split level pulse	2.71	2	2
Conventional CMOS	3.27	2	1
2n2p-2n	3.45	6	1
REL in MOSFETs	5.74	4	1
2n-2n2p quasi	5.77	6	1

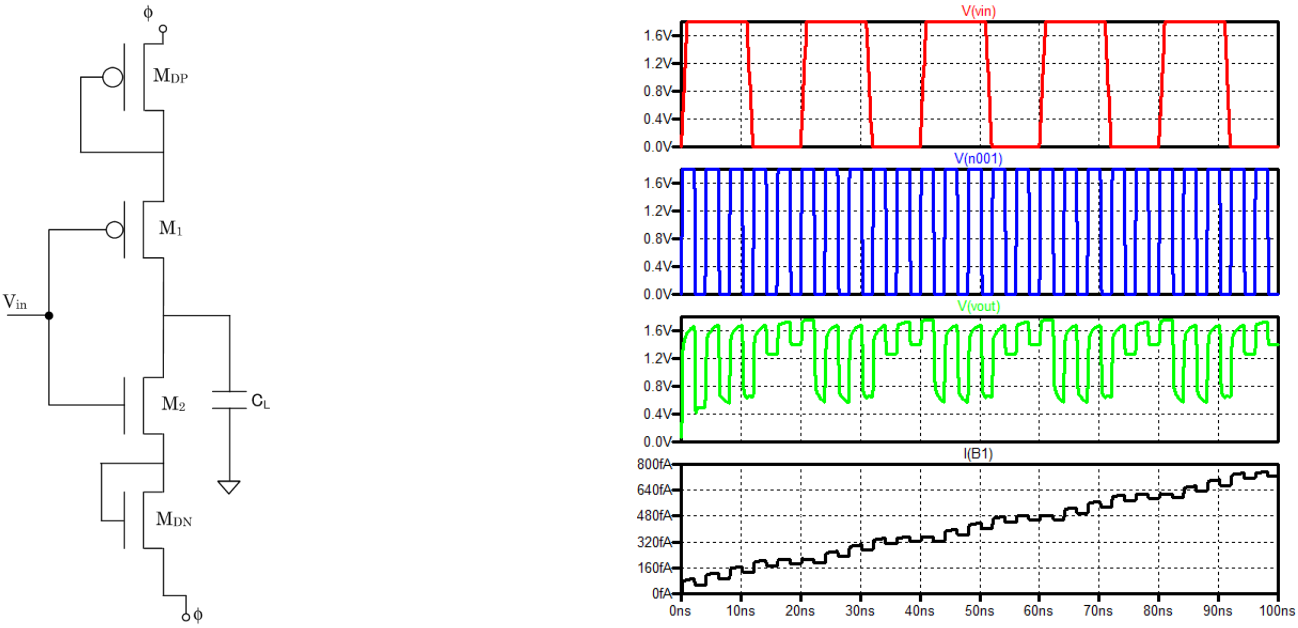

Fig. 11 Modified Adiabatic Dynamic CMOS logic (ADCL) circuits diagram and waveforms

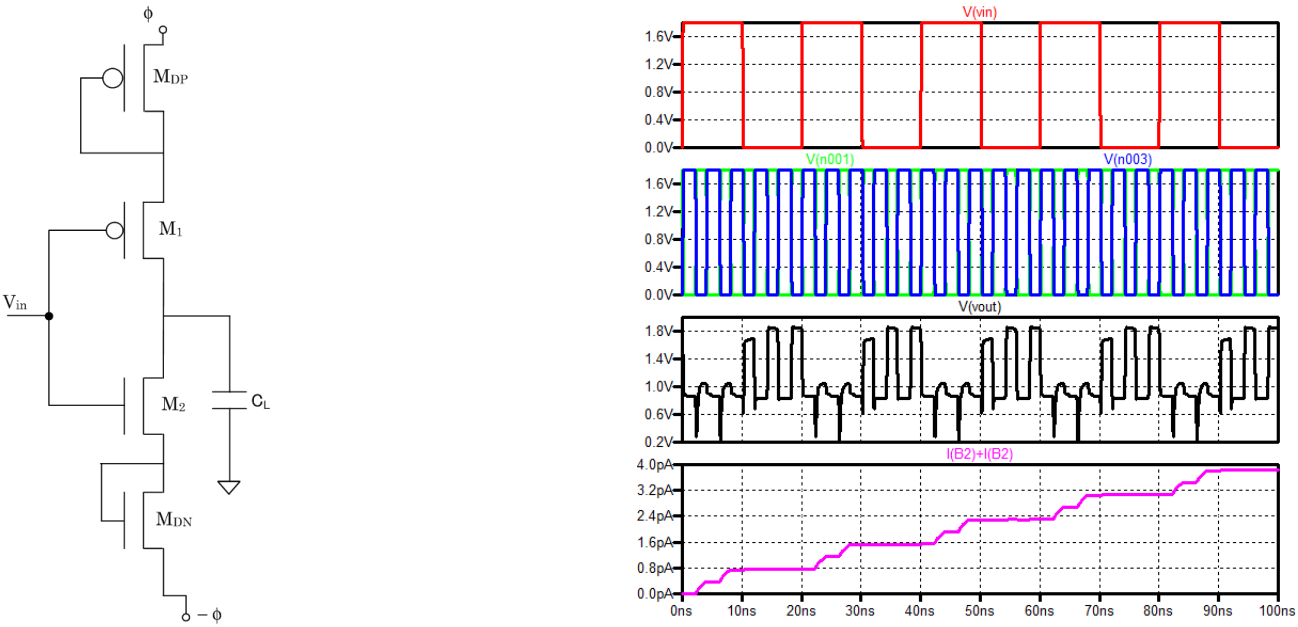

Fig. 12 Two-phase drive adiabatic dynamic CMOS logic (2PADCL) circuits diagram and waveforms

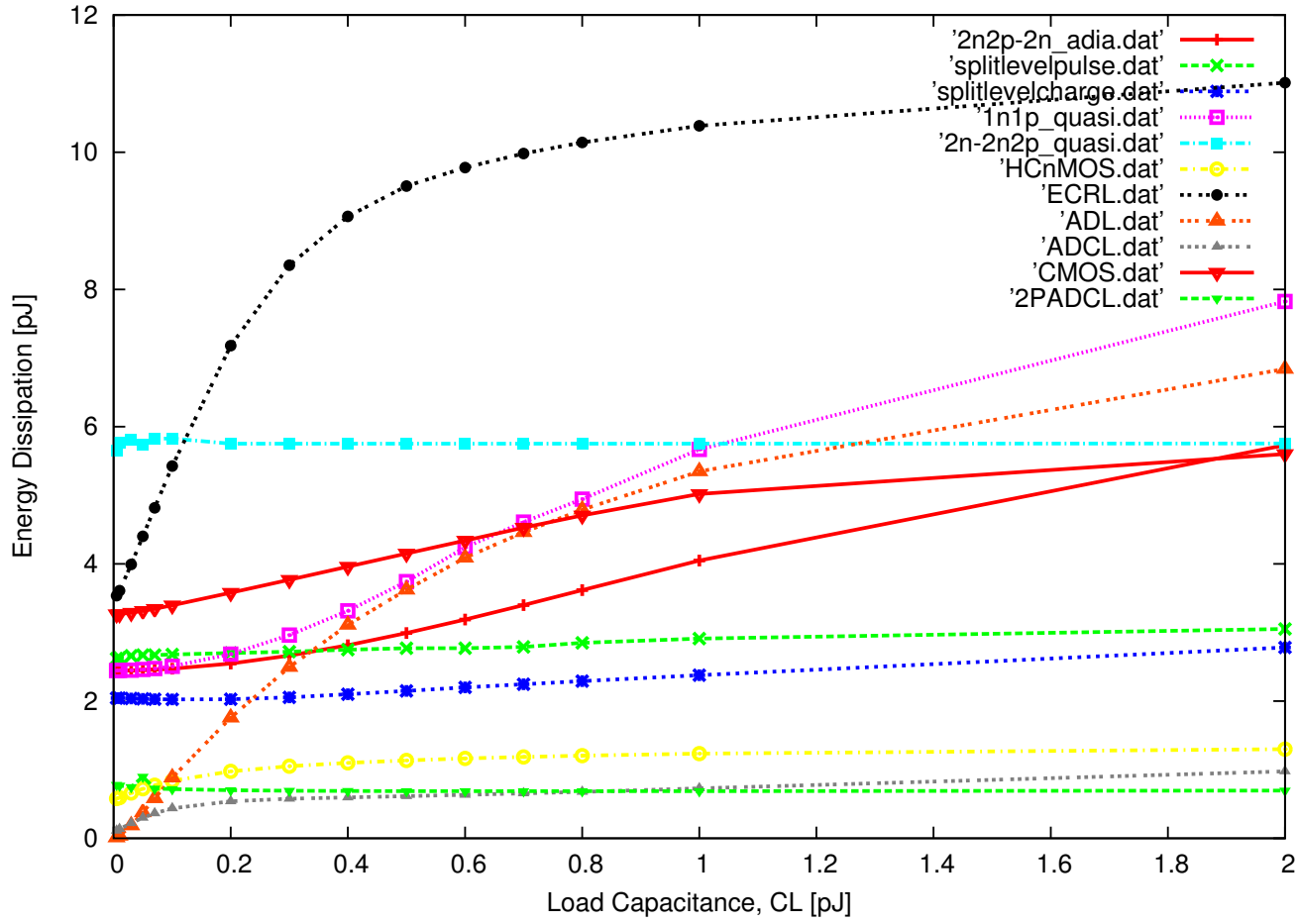

Fig. 13 Energy dissipation comparison in adiabatic circuits at different load capacitance value