2PASCL: Energy dissipation at different input transition and pulse driving voltage

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Abstract

This paper proposes a new quasi adiabatic logic family that uses two complementary pulsed supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the chain of four 2PASCL inverters implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. This circuit is emphasis on the recycle of the charges as two diodes are placed for the discharging. The ealier results show that 2PASCL can save a maximum of 63.3% of power dissipation over static CMOS logic at transition frequencies of 50MHz to 100MHz.

Introduction

In the previous simulation, we understood that four chain inverters of 2PASCL (Fig.1) at 125 MHz clocking voltage show a significant lower result than CMOS from 10 to 100 MHz transition frequency. The higher the clocking voltage the higher energy dissipation. In this simulation we compared the results of the different transition frequency values to the clocking voltage pulse. We would like to examine the minimum clocking power pulse needed for an input pulse for an efficient energy recovery.

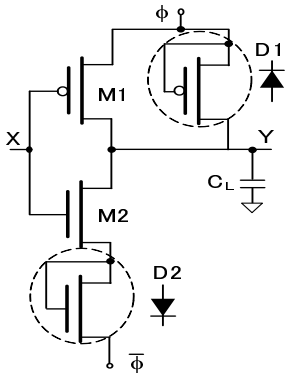

Fig. 1 2PASCL inverter circuit.

Simulation and results

The simulation of four chain 2PASCL inverter circuit as in schematic diagram and the output results shown in Fig. 2 has been done.Its function is evaluated using the output waveforms graph. At input frequency of 10 to 300MHz, power dissipation per cycle comparison to static CMOS chain inverter is as demonstrated in Fig. 3. Lower clock voltage frequency gives a lower power dissipation, P. P increases with the increasing transition frequency, f. In Fig. 4, we rearrange the data by eliminating the circuits that are not functioning as inverters after increasing the input voltage. Then, the clocking speed is at least 2 times higher than the input frequency, while in Fig. 5, the speed is 3 times higher. In Fig. 6, we run another simulation to see the characteristic when the clocking voltage frequency is the exact multiplication of the input frequency at 2, 3, 4, 5 and 10 times. From the graph, we knows that at least 4 times input pulse frequency can give a better result. Results are also compared to 2PADCL at 200 MHz clocking voltage. Here, 2PADCL shows a lower result.

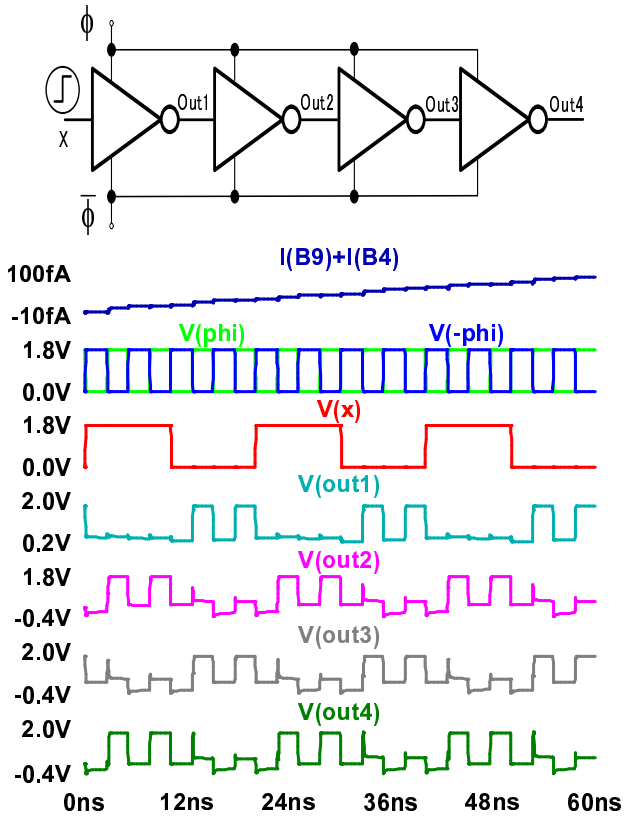

Fig. 2 2PASCL chain inverter circuit and simulation results where clocking volatage is 4 times higher than the input signal.

Conclusion

In this simulation we have confirmed the functional operation of four chain diodes and the result shows that a minimum of 4 times of the clocking voltage pulse frequency to the input frequency can give a lower energy dissipation at relatively up to 200 MHz input frequency.

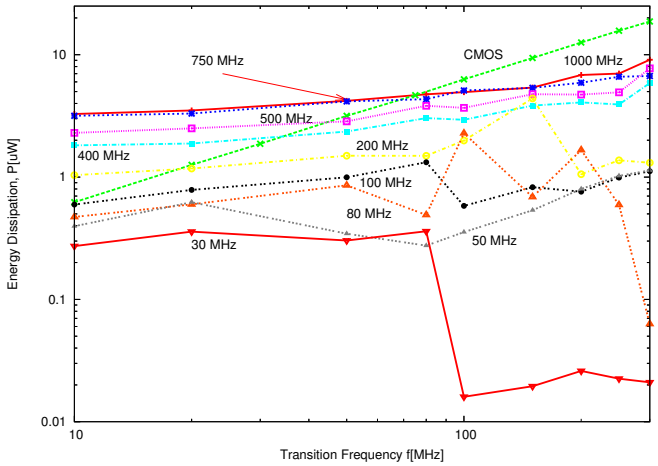

Fig. 3 Power dissipation at different transition frequency.

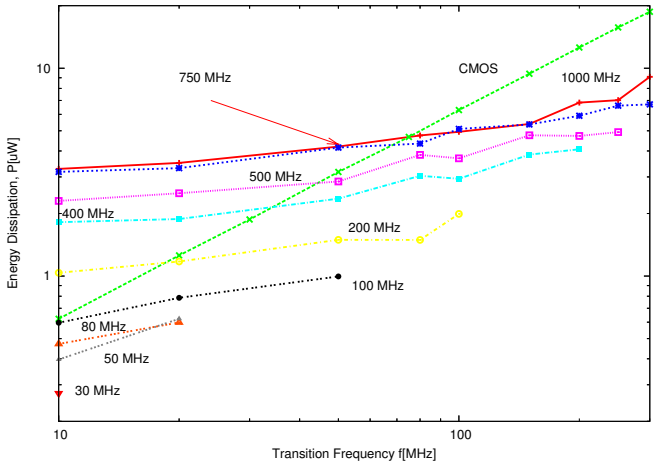

Fig. 4 Power dissipation at different transition frequency minimum clocking signal is 2 times faster than the input signal.

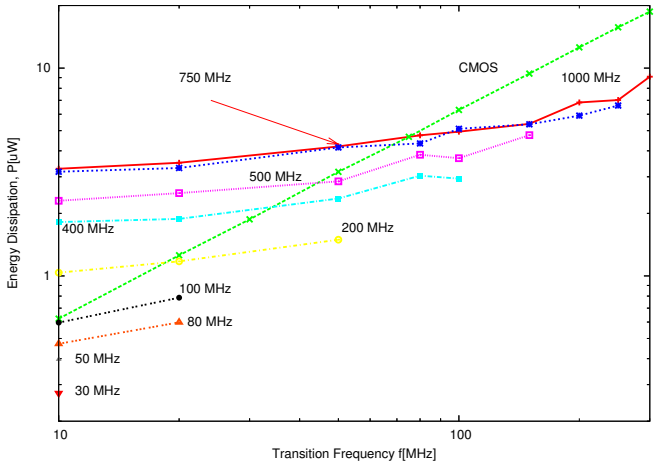

Fig. 5 Power dissipation at different transition frequency where minimum clocking signal is 3 times faster than input signal.

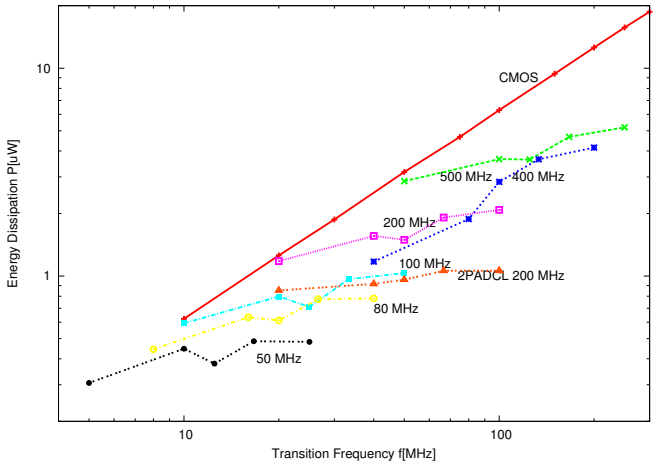

Fig. 6 Power dissipation at different transition frequency where the multiplication of the input frequency is the exact value of the clocking voltage and also comparison to 2PASCL @200 MHz and CMOS.