# 2PASCL: Energy dissipation of NAND circuit and simulation with trapezoidal and sine voltage clocking power

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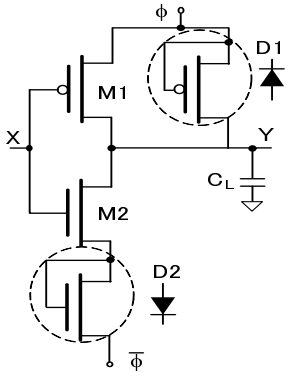
**Abstract**

This paper proposes a new quasi adiabatic logic family that uses two complementary pulsed supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL NAND implemented using 0.18 $\mu$m CMOS technology. Driving pulse with the height equal to $V_{dd}$ is supplied to the gates. This circuit is emphasis on the recycle of the charges as two diodes are placed for the discharging. The ealier results show that 2PASCL can save a maximum of 63.3% of power dissipation over static CMOS logic at transition frequencies of 50MHz to 100MHz.

## 1 Introduction

In the previous simulation, we have confirmed the functional operation of four chain inverters and the result shows that a minimum of 4:1 of the clocking voltage pulse frequency to the input frequency can give a lower energy dissipation at relatively up to 200 MHz input frequency. In this simulation we will continue simulation with NAND circuit using 2PASCL circuit. The input waveforms used are pulse, trapezoidal and sinusoidal. The result will be compared to static CMOS NAND and 2PADCL which uses trapezoidal clocking voltage power waveforms. The 2PASCL circuit diagram and its truth table are shown in Fig. 1.




| X | $\phi$ | Y |
|---|---|---|
| 1 ⟶ 0 | $V_\phi$ → Hi | $V_\phi$ |
| | $V_\phi$ → Lo | $V_\phi$ |
| 0 ⟶ 1 | $V_{\overline{\phi}}$ → Hi | $V_t$ |
| | $V_\phi$ → Lo | $V_t$ |

Fig. 1 2PASCL inverter circuit and its truth table

## 2 Simulation and results

The simulation of 2PASCL NAND circuit as in schematic diagram shown in Fig. 2 has been done. The differences compared to static CMOS NAND circuit are two diodes placed near the output and next to the nMOS logic and clocking voltage power supply to replace the $V_{dd}$ and the ground. Its function is evaluated using the output waveforms graph. Then by using the SPICE simulation, the energy dissipation for one cycle is calculated. The energy in joule is then converted to watt by multiplying it with the input frequency.

At circuit condition shown in Table 1, energy dissipation per cycle is compared to 2PADCL which is using trapezoidal voltage clocking and static CMOS NAND circuit. At low input frequency of 10 MHz, CMOS shows the lowest energy dissipation followed by 2PADCL with trapezoidal waveforms clocking voltage. 2PADCL is followed closely by 2PASCL with trapezoidal clocking. Next is 2PASCL with pulse and the highest energy dissipation is demonstrated by the 2PASCL sinusoidal clocking voltage power.

Table 1 Comparison of Energy Dissipation

| | |
|---|---|
| Input a | pulse, $T_{on}$: 50n, $freq$ 10MHz, delay: 50n |
| Input b | pulse, $T_{on}$: 100n,$freq$ 5MHz, delay: 100n |
| $C_L$ | 0.1 pF |
| Diodes | W/L : 30$\mu$m/0.18$\mu$m |
| nMOS, pMOS | W/L : 0.6$\mu$m/0.18$\mu$m |

### 2.1 Clocking voltage power condition

- Pulse
  - $\phi$ $V_{init}$=0V, $V_{on}$=1.8V, delay=6.25n, $T_{rise}/T_{fall}$=0.01n, $T_{on}$=12.5n, $T_{period}$=25n
  - $\overline{\phi}$ $V_{init}$=1.8V,$V_{on}$ 0V, delay=6.25n, $T_{rise}/T_{fall}$=0.01n, $T_{on}$=12.5n, $T_{period}$=25n
- Trapezoidal
  - $\phi$ $V_{init}$=0V, $V_{on}$=1.8V, delay=6.25n, $T_{rise}/T_{fall}$=3n, $T_{on}$=12.5n, $T_{period}$=25n
  - $\overline{\phi}$ $V_{init}$= 1.8V,$V_{on}$=0V, delay=6.25n, $T_{rise}/T_{fall}$=3n, $T_{on}$=12.5n, $T_{period}$=25n
- Sinusoidal
  - $\phi$ amplitude=1.8V, $f$=40MHz, delay=-6.25n
  - $\overline{\phi}$ amplitude=-1.8V, $f$=40MHz, delay=-6.25n

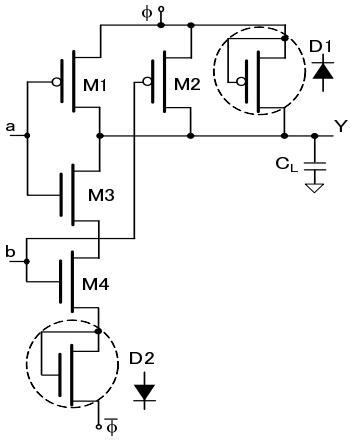



Fig. 2 NAND logic circuit with 2PASCL configuration.

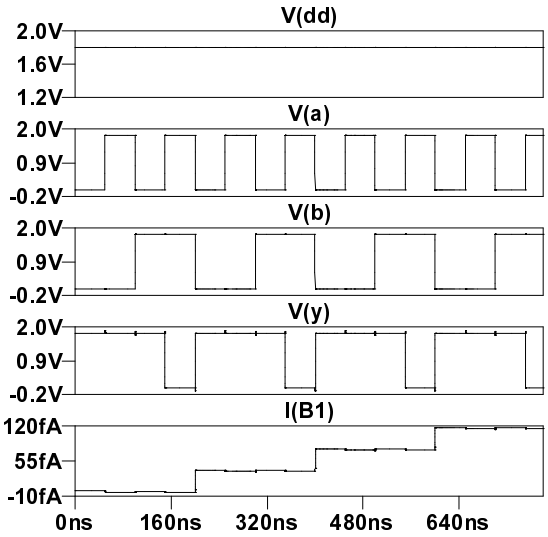



Fig. 3 NAND logic circuit using static CMOS.

Table 2 Comparison of Energy Dissipation of NAND circuit

| Config. | Waveform | E($\mu$W/cycle) | Gates | Drivers |
|---|---|---|---|---|
| CMOS | $V_{dd}$ | 0.3887 | 4 | 1 |
| 2PADCL | trapezoidal | 7.3378 | 6 | 2 |
| 2PASCL | trapezoidal | 8.4755 | 6 | 2 |
| 2PASCL | pulse | 14.2138 | 6 | 2 |
| 2PASCL | sinusoidal | 31.336 | 6 | 2 |

## 3 Conclusion

From this simulation, the functional of 2PASCL as NAND logic circuit has been confirmed. The energy dissipation is higher than static CMOS at 10 MHz transition frequency. In terms of clocking voltage clocking, trapezoidal waveforms showed a lower energy dissipation compared to pulse and sinusoidal waveforms.

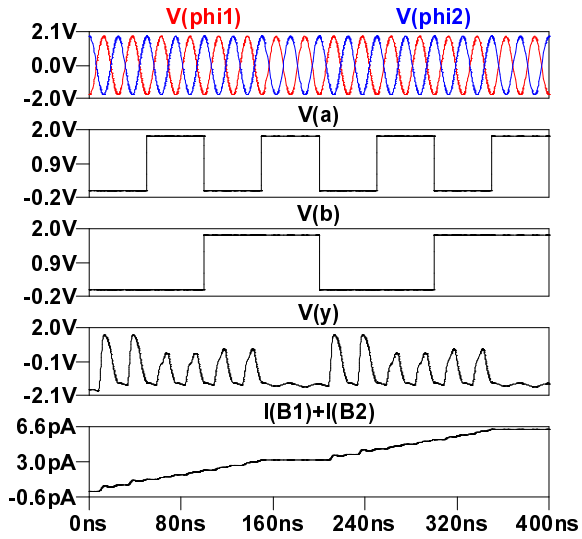



Fig. 4 NAND logic circuit using 2PASCL showing input, output waveforms and energy dissipation using sine waveform as clocked voltage driving.

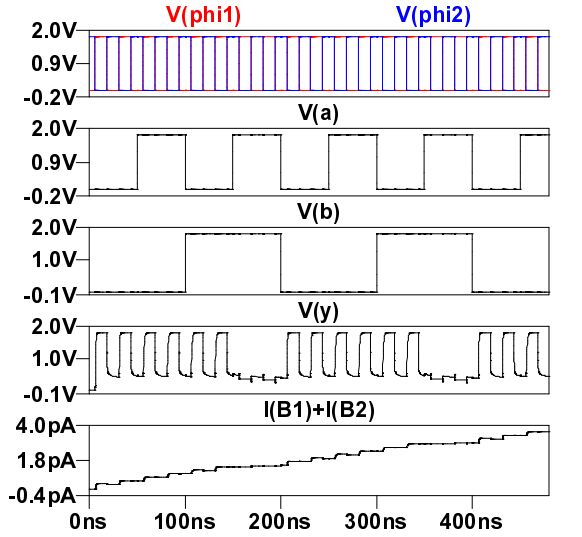



Fig. 5 NAND logic circuit using 2PASCL showing input, output waveforms and energy dissipation using pulse waveform as clocked voltage driving.

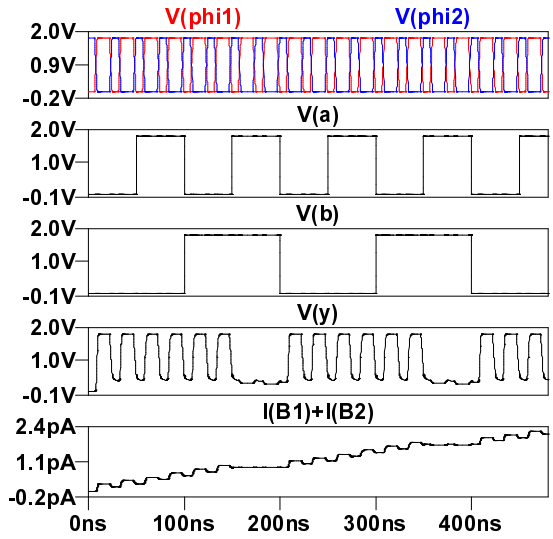



Fig. 6 NAND logic circuit using 2PASCL showing input, output waveforms and energy dissipation using trapezoidal waveform as clocked voltage driving.

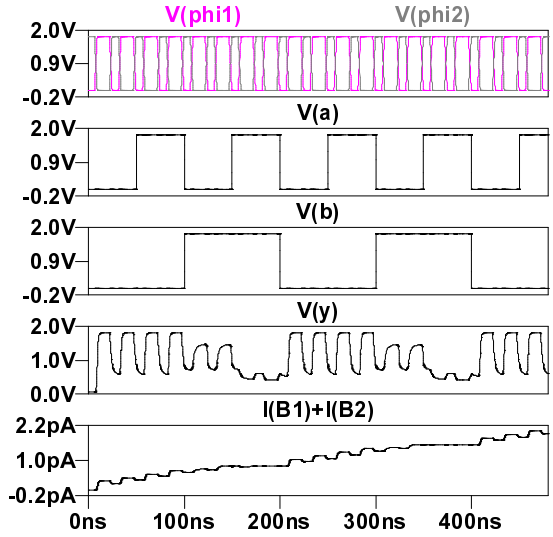



Fig. 7 NAND logic circuit using 2PADCL showing the input, output waveforms and energy dissipation using trapezoidal waveform as clocked voltage driving.