2PASCL: Energy dissipation of NOR gate and exclusive-OR gate circuit using sinusoidal split level driving voltage

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Abstract

This paper proposes a new quasi adiabatic logic family that uses two complementary sinusoidal supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL logic gates implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. This circuit is emphasized on the recycle of the charges as two diodes are placed for the discharging. The earlier results of inverter logic, it shows that 2PASCL can save a maximum of 82.5% of power dissipation over static CMOS logic at transition frequency of 100MHz.

1 Introduction

The first difference of 2PASCL compared to static CMOS logic gate is two diodes, one from the output node to the clocking voltage and another one is placed next to the nMOS logic to another clocking voltage. The next difference is that sinusoidal clocking voltage is used to replace the V_{dd} and the GND. By using the SPICE simulation, the energy dissipation for one logic cycle is calculated. The energy in joule is then converted to watt by multiplying it with the input frequency.

In the previous simulation, we found that split level sinusoidal dissipates lower energy compared to trapezoidal driving voltage. This is just the opposite when using the two phase inverted sinusoidal driving pulse. By using split level driving voltage and nMOS bulks connected to the $\overline{\phi}$ and pMOS bulks to ϕ, we managed to produce a better output waveforms and significantly lower energy dissipation. The result shows a maximum of 30.5% lower energy dissipation when using 2PASCL NAND logic compared to static CMOS NAND logic with the V_{dd} of 1.8V. The delay time from input to output measured as 1.28 ns.

In this paper, we are going to simulate 2PASCL NOR and exclusive-OR gates using split level sinusoidal driving voltage. Bulks will be connected to $\overline{\phi}$ and ϕ. Comparison of the energy dissipation to conventional static CMOS logic with V_{dd} of 1.8V will be carried out. The transition frequency simulated will be from 10 to 100 MHz. We will also summarize all the 2PASCL gates and its energy dissipation to CMOS.

2 Simulation and results

The simulation of 2PASCL NOR and exclusive-OR gates as in schematic diagram shown in Fig. 3– Fig. 4 is carried out. We use sinusoidal split driving voltage ranging from 0 to 1.8V. The circuit condition is as shown in Table 1. By taking one transition frequency of 100 MHz, the functional of the NOR and exclusive-OR are confirmed from Fig. 5 and Fig. 6. Then, the simulation result for the transition frequency of 10, 20, 40, 80 and 100 MHz is compared to the same frequency of CMOS static logic circuits. The result is as shown in Fig.7– Fig. 8. From the results, 2PASCL with split level sinusoidal clocking voltage gives a significant lower energy dissipation compared to conventional static CMOS.

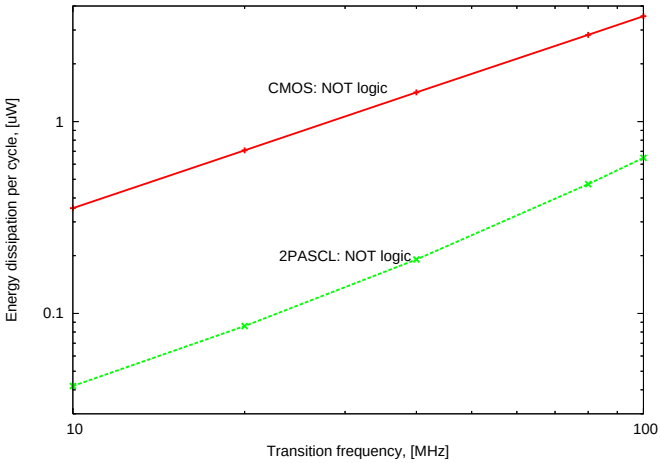

Fig. 1 Energy dissipation of 2PASCL NOT logic circuit compared to CMOS.

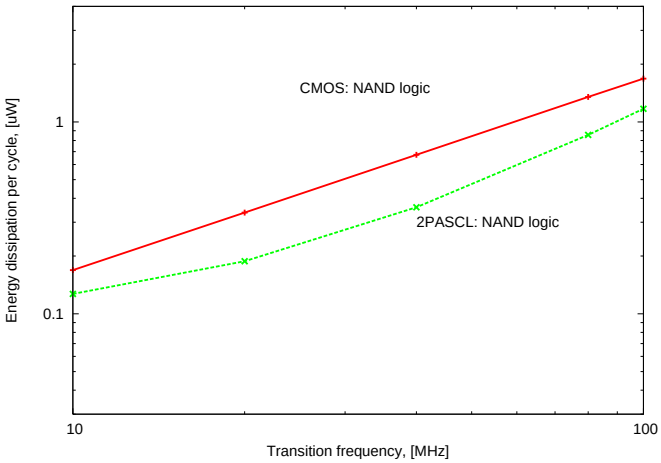

Fig. 2 Energy dissipation of 2PASCL NAND logic circuit compared to CMOS.

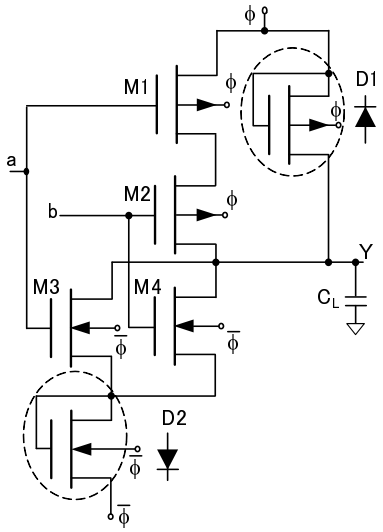

Fig. 3 NOR logic circuit with 2PASCL configuration. nMOS bulk connected to $\overline{\phi}$ and pMOS bulk to ϕ.

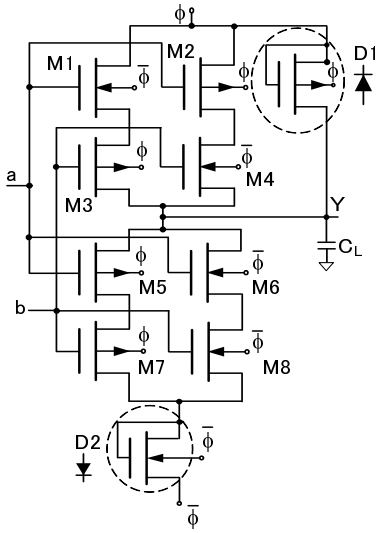

Fig. 4 exclusive-OR logic circuit with 2PASCL configuration. nMOS bulk connected to $\overline{\phi}$ and pMOS bulk to ϕ.

Table 1 Circuit data for sinusoidal and static CMOS comparison

Driving power voltage	0–1.8V
Split level	0–0.9V, 0.9–1.8V
Freq, (input: driving voltage)	1:4
C_L	0.01 pF
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm

3 Conclusion

In this simulation, same as previously done NAND logic, sinusoidal using split level dissipates lower energy compared static CMOS for NOR and exclusive-OR logic. At 100 MHz, NOR and exclusive-OR are 25.8% and 67.8% lower when using 2PASCL logic compared to static CMOS NAND logic with the V_{dd} of 1.8V.

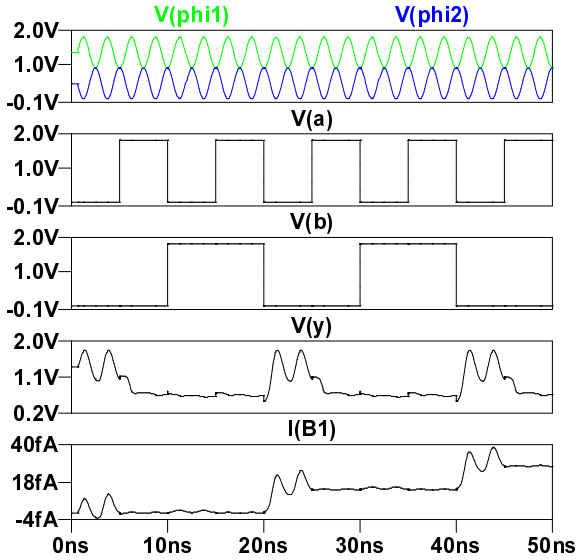

Fig. 5 2PASCL NOR logic circuit with sinusoidal driving voltage.

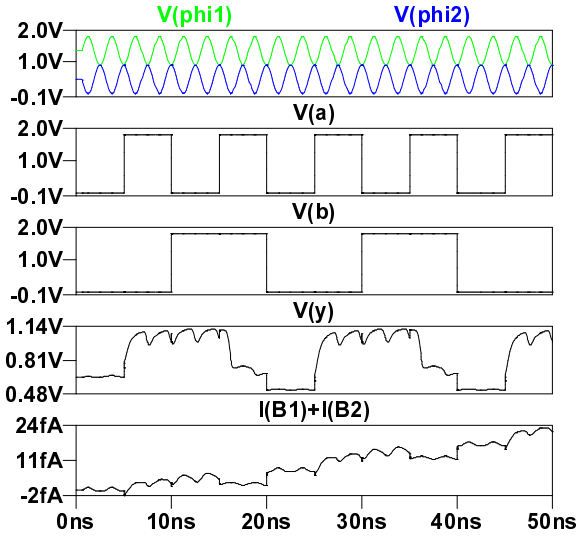

Fig. 6 2PASCL exclusive-OR logic circuit with sinusoidal driving voltage.

Table 2 Energy dissipation per cycle difference

	CMOS [μW]	2PASCL[μW]	Diff @100 MHz [%]
NOT	3.54	0.617	82.5
NAND	1.68	1.17	30.4
NOR	1.86	1.38	25.8
XOR	2.90	0.932	67.8

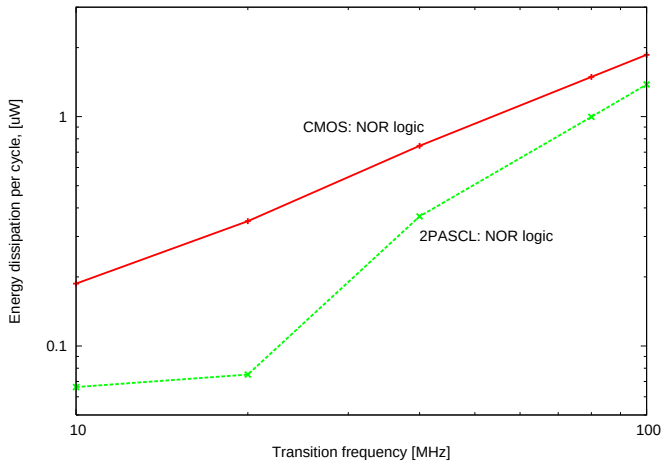

Fig. 7 2PASCL NOR logic circuit with sinusoidal driving voltage.

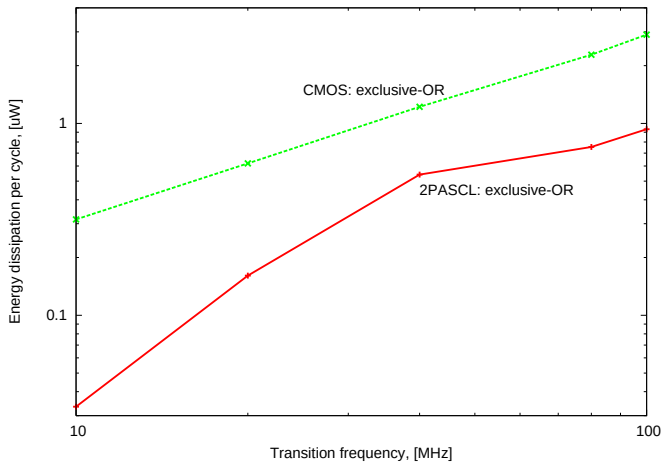

Fig. 8 2PASCL exclusive-OR logic circuit with sinusoidal driving voltage.