Energy dissipation comparison: 2PASCL versus CMOS for 2 input multiplexer (2:1MUX) and 1-bit full adder (FA)

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Abstract

The paper presents a new quasi energy recovery logic family that uses two complementary split-level sinusoidal power supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) is using the principle of adiabatic switching. It has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL logic gates implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. For an inverter and four-inverter chain, it shows that 2PASCL can save 82.6% and 56.9% of energy respectively over static CMOS logic at transition frequency of 100MHz.

1 Introduction

We propose a two phase adiabatic static CMOS logic (2PASCL) circuit. It can be directly converted from static CMOS circuits without drastically increasing the circuit complexity and transistor overheads. This circuit is emphasized on the recycle of the charges as two diodes are placed for the discharging. Energy dissipations for inverter, four-inverter chain, NAND, NOR and exclusive-OR logic circuits based on 2PASCL are compared to CMOS at transition frequency of 10 to 100 MHz. We also simulate the effects of the load capacitance to the energy dissipation and a comparison to other adiabatic inverter circuits.

2 Two Phase Adiabatic Static CMOS Logic

Figure 1 shows a circuit diagram and waveforms illustrating the operation of the 2PASCL inverter. It resembles the static CMOS logic inverter but operates in a nearly adiabatic fashion. The first difference of 2PASCL compared to static CMOS logic gate is the two diodes, one from the output node to the power clock supply and another one is placed next to the nMOS logic to another power clock. The pMOS and nMOS diodes are used to recycle the charge from the output node. The other difference is that split-level sinusoidal power clock supplies, ϕ and $\overline{\phi}$ are used to replace the V_{dd} and the GND. From the simulation, we found that split-level sinusoidal gives a lower energy dissipation compared to trapezoidal power clock supply even if we set the T_{rise} and T_{fall} of the trapezoidal waveforms to a maximum values. By using two split-level sinusoidal waveforms which peak-to-peak are 0.9 V, we can reduced the voltage difference, thus reducing the charging and discharging activities. Sinusoidal waveforms can also be generated with higher energy efficiency than trapezoidal waveforms.

The operation of 2PASCL is as follows. Let us consider the inverter logic circuit demonstrated in Fig. 1. The circuit operation phase is divided into *evaluation* and *hold*.

In *evaluation* phase, when the output node Y is LOW and pMOS tree is turned ON, as ϕ swings up and $\overline{\phi}$ swings down, C_L is charged through pMOS transistor resulting the HIGH state at Y. When Y is LOW and nMOS is ON, no transition occurs. The same result gained when Y is HIGH and pMOS is ON. When Y is HIGH and nMOS is ON, discharging via nMOS and D2 resulting the output voltage decreased to V_t value before entering *hold* mode where the logical state is '0'. For the *evaluation* mode where ϕ swings up and $\overline{\phi}$ swings down, the operation could be summarized by Table 1.

Table 1 Operation summary at evaluation mode

Prelim. state Y	ON transistor	Next state of Y
LOW	M1	HIGH
LOW	M2	LOW (no transition)
HIGH	M1	HIGH (no transition)
HIGH	M2	LOW

At *hold* mode where ϕ swings down and $\overline{\phi}$ swings up, due to the diodes, the state of Y when preliminary state is LOW remains unchanged. When the preliminary state of Y is HIGH, it will change to V_t, the threshold voltage of the diode. At this point, discharging via D1 occurs.

From the operation of 2PASCL, less dynamic switchings are seen as circuit nodes are not necessarily charging and discharging every clock cycle which reduces the node switching activities significantly. The lower the switching activity reduces energy dissipation.

In the previous simulation, same as NAND logic, sinusoidal using split level dissipates lower energy compared static CMOS for NOR and exclusive-OR logic. At 100 MHz, NOR and exclusive-OR are 25.8% and 67.8% lower when using 2PASCL logic compared to static CMOS NAND logic with the V_{dd} of 1.8V.

In this paper, we are going to simulate a two input multiplexer as its schematic shown in 2 and 1 bit full adder of 2PASCL as in 4 using split level sinusoidal driving voltage. Bulks will be connected to $\overline{\phi}$ and ϕ. Comparison of the energy dissipation to conventional

static CMOS logic with V_{dd} of 1.8V will be carried out.

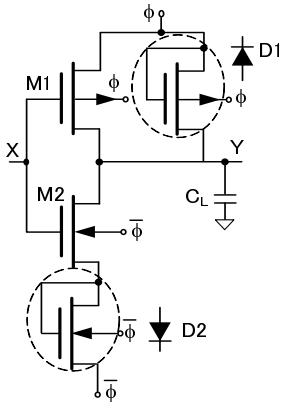

Fig. 1 2PASCL inverter logic circuit.

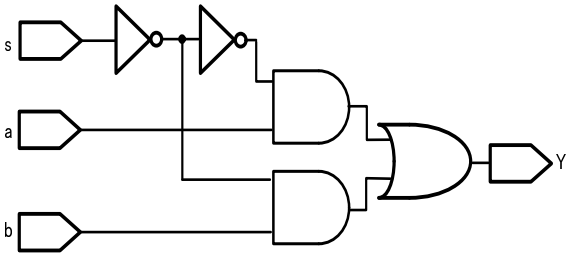

Fig. 2 Schematic circuit of two-input multiplexer where Y=(a·s) + (b·$\overline{s}$).

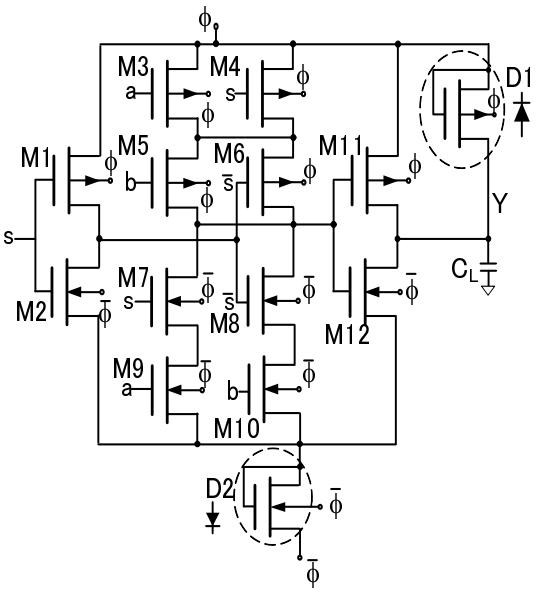

Fig. 3 Lay-out of two-input multiplexer of 2PASCL.

3 Simulation and results

The simulation of 2PASCL 2:1 MUX and full adder as in layout shown in Fig. 3 and Fig. 5 is carried out. We use sinusoidal split driving voltage ranging from 0 to 1.8V. The circuit condition is as shown in Table 2. The functional of the 2:1 MUX and full adder are

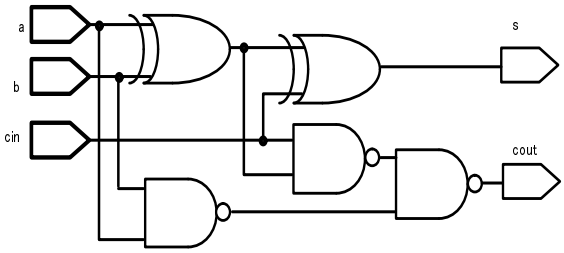

Fig. 4 Schematic circuit of one bit full adder.

confirmed from Fig. 6 – Fig. 9. Then, the simulation result for the transition frequency of 5 MHz for 2:1 MUX and 16.7 MHz are compared to the same frequency of CMOS static logic circuits. The result is as shown in Fig.6– Fig. 9. From the results, 2PASCL with split level sinusoidal clocking voltage gives a significant lower energy dissipation compared to conventional static CMOS.

Table 2 Circuit data for sinusoidal and static CMOS comparison

Driving power voltage	0–1.8V
Split level	0–0.9V, 0.9–1.8V
Freq, (input: driving voltage)	1:4
C_L	0.01 pF
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm

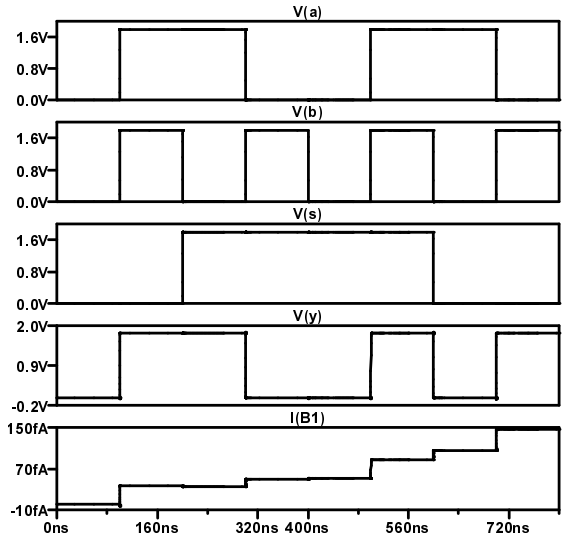

Fig. 6 2:1 MUX CMOS simulation results.

4 Conclusion

In this simulation, two input multiplexer and 1 bit full adder of 2PASCL show 71.4% and 80.5% lower energy dissipation at input frequency of 5 MHz and 16.7 MHz respectively compared to static CMOS..

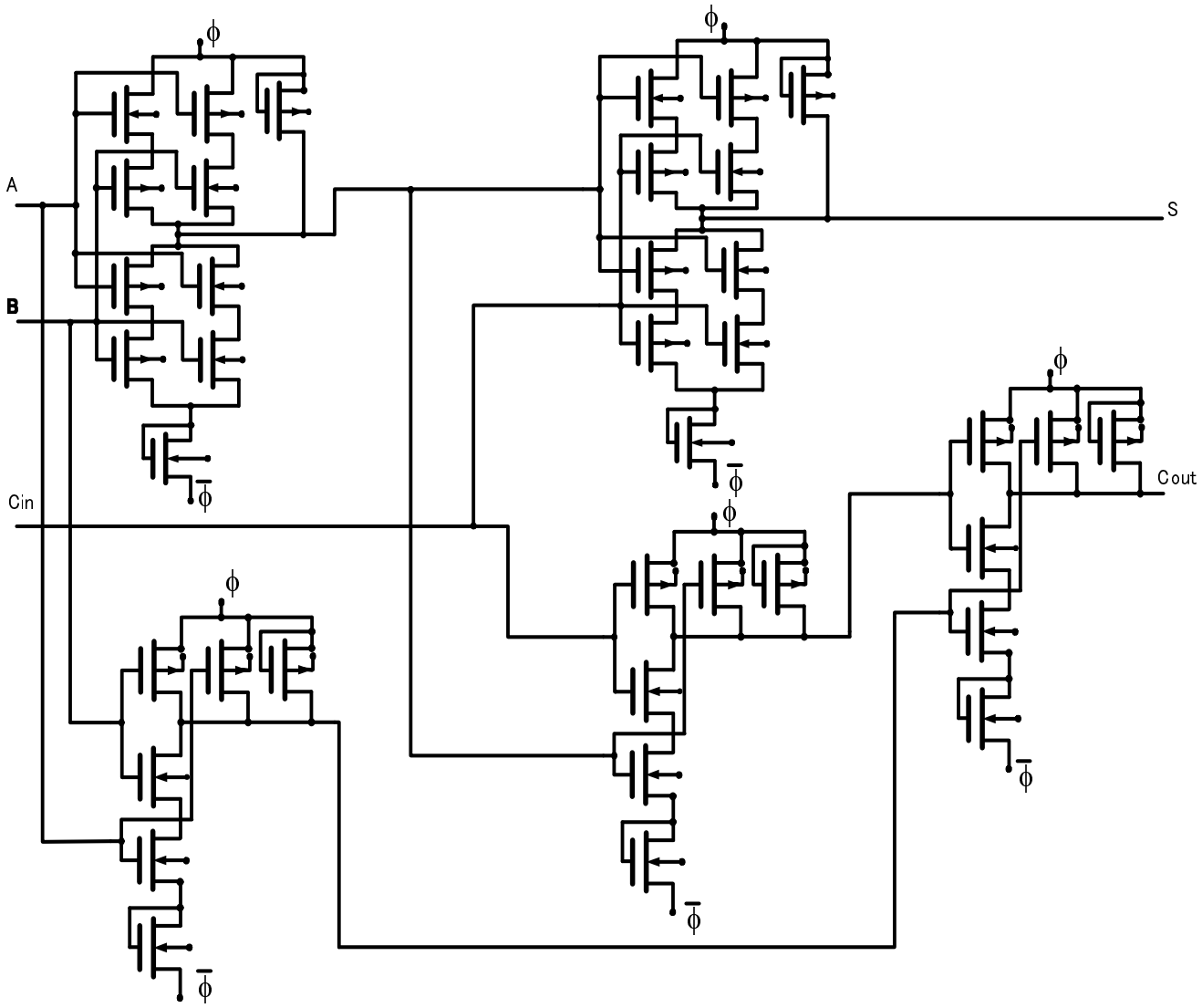

Fig. 5 Full adder for 2PASCL layout.

Table 3 Energy dissipation per cycle difference

	CMOS [fJ]	2PASCL[fJ]	Diff [%]
2:1 MUX (@ 5 MHz)	145.9	41.8	71.4
Full Adder (@ 16.7 MHz)	240	46.8	80.5

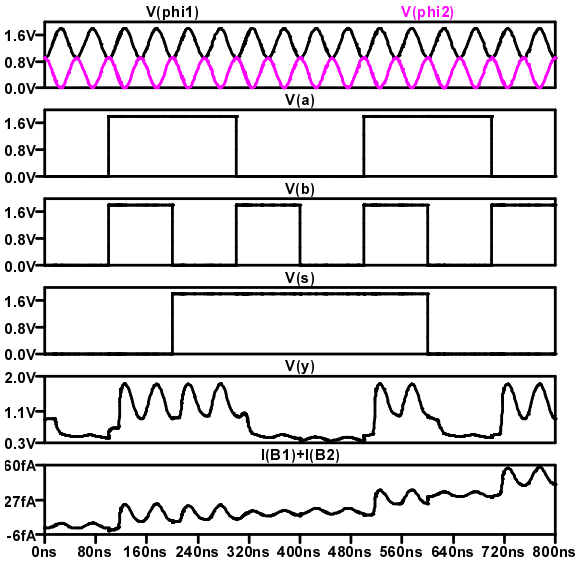

Fig. 7 2:1 MUX 2PASCL simulation result.

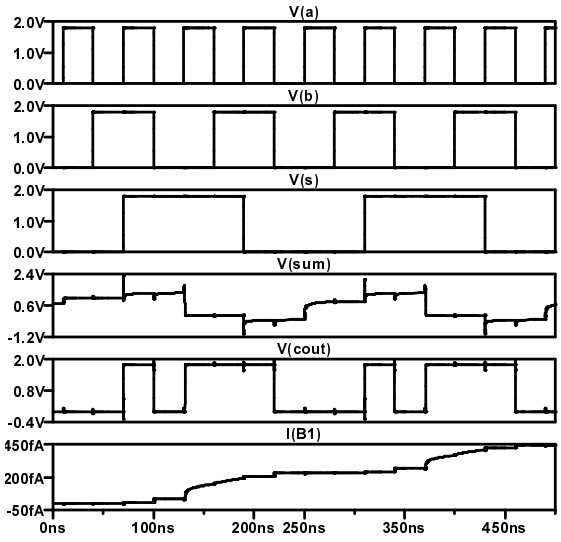

Fig. 8 Full adder CMOS simulation result.

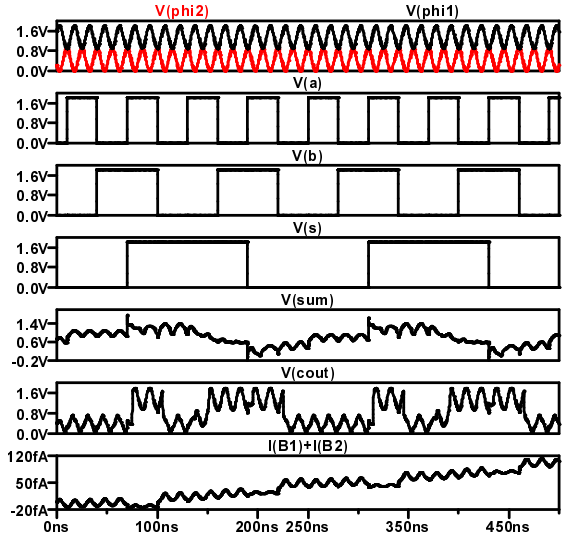

Fig. 9 Full adder 2PASCL simulation result.