1-bit full adder (FA) with new exclusive-OR of 2PASCL and introduction to 2PASCL Ripple Carry Adder (RCA)

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Abstract

The paper presents a new quasi energy recovery logic family that uses two complementary split-level sinusoidal power supply clock for digital low power applications such as sensors. The proposed two-phase adiabatic static CMOS logic circuit (2PASCL) is using the principle of adiabatic switching. It has switching activity that is lower than dynamic logic and can be directly derived from static CMOS circuits. We have done a SPICE simulation on the 2PASCL logic gates implemented using 0.18 μm CMOS technology. Driving pulse with the height equal to V_{dd} is supplied to the gates. For an inverter and four-inverter chain, it shows that 2PASCL can save 82.6% and 56.9% of energy respectively over static CMOS logic at transition frequency of 100MHz.

1 Introduction

In the previous simulation, two input multiplexer and 1 bit full adder of 2PASCL show 71.4% and 80.5% lower energy dissipation at input frequency of 5 MHz and 16.7 MHz respectively compared to static CMOS. However we found that the output waveforms of the full adder is not properly differentiate the HIGH and LOW value especially at the SUM output.

In this paper, we redesign the exclusive-OR of 2PASCL which consist of 15 transistoirs including the inverters and diodes and compared with exclusive-OR CMOS which consist only 6 transisors. Then, we again combine it with the NAND circuit to create full adder (FA) combination circuit. Comparison with CMOS FA in term of energy dissipation is carried out. Next, we introduce the ripple carry adder (RCA) of 2PASCL by showing the output waveforms.

2 Simulation and results

By using split level driving voltage sinusoidal ranging from 0 to 1.8V, simulations of new exclusive-OR 2PASCL and CMOS which schematic shown in Fig. 1 and Fig. 3 are carried out. The results and the functional confirmation are shown in Fig. 2 and Fig. 4. Bulks are connected to ϕ and $\overline{\phi}$. The circuit condition is as shown in Table 1

By using this new schematic full adder which consist of exclusive-OR and NAND logics is simulated for 2PASCL (Fig. 5) and CMOS. The results are shown in Fig. 6 and Fig. 7. Comparison of the energy dissipation for the transition frequency of 16.67 MHz with conventional static CMOS logic with V_{dd} of 1.8V is shown in Table 2. From the results, 2PASCL with split level sinusoidal clocking voltage gives a significant lower energy dissipation compared to conventional static CMOS in both single exclusive-OR logic and full adder (FA) even though the number of transistor in 2PASCL is 15 compared to only 6 in CMOS exclusive-OR. Next, we present the 2PASCL ripple carry adder (RCA) as shown in Fig. 8 and its result in Fig. 6.

Table 1 Circuit data for sinusoidal and static CMOS comparison

Driving power voltage	0–1.8V
Split level	0–0.9V, 0.9–1.8V
Freq, (input: driving voltage)	1:4
C_L	0.01 pF
Diodes	W/L : 0.6μm/0.18μm
nMOS, pMOS	W/L : 0.6μm/0.18μm

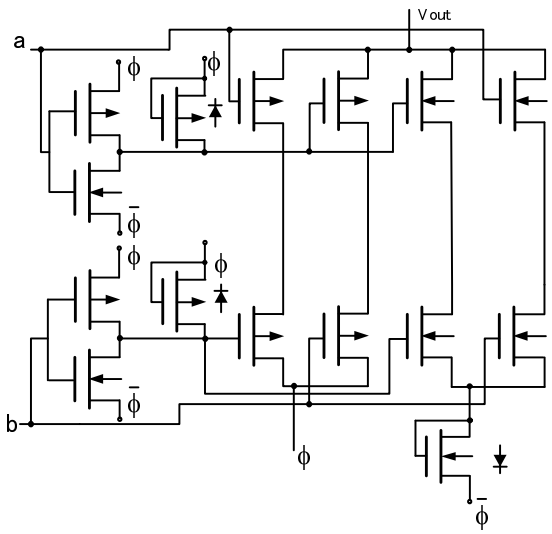

Fig. 1 New schematic for exclusive-OR of 2PASCL.

Table 2 Energy dissipation per cycle difference

	CMOS [fJ]	2PASCL[fJ]	Diff [%]
ex-OR (@ 16.67 MHz)	19.48	15.52	19.8
Full Adder (@ 16.67 MHz)	359	256	21.7

3 Conclusion

In this simulation, 1 bit full adder of 2PASCL shows 21.7% lower energy dissipation at input frequency of 16.7 MHz compared to static CMOS.

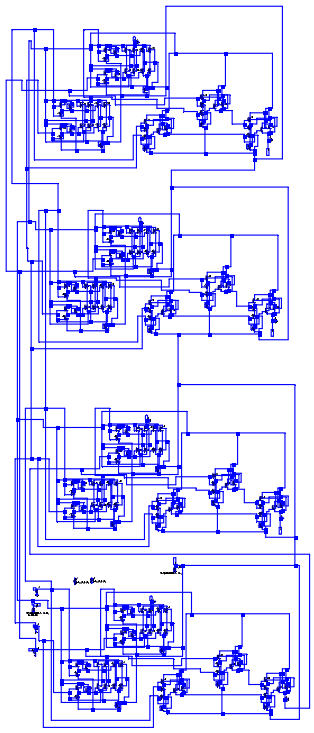

Fig. 8 Schematic of ripple carry adder (RCA) 2PASCL.

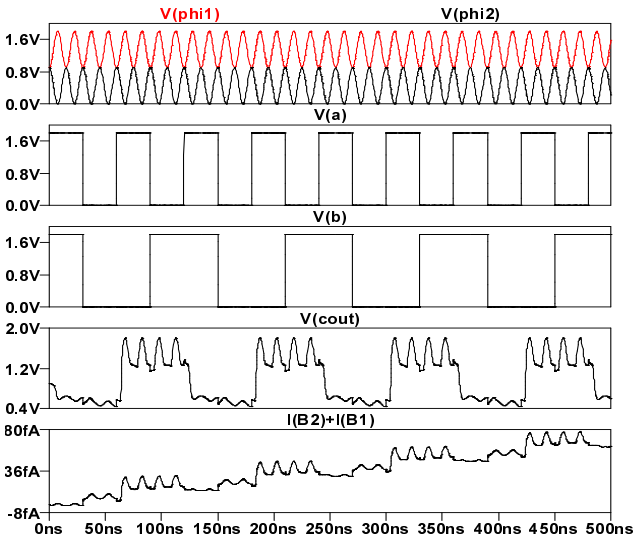

Fig. 2 New schematic for exclusive-OR of 2PASCL waveforms.

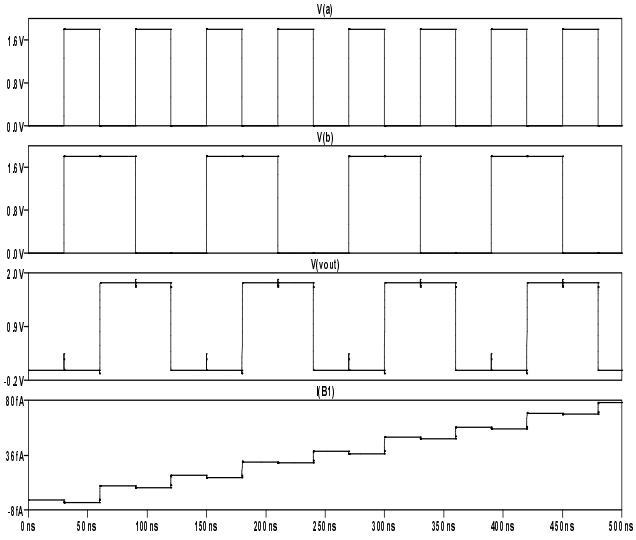

Fig. 4 Waveforms for new schematic for exclusive-OR CMOS.

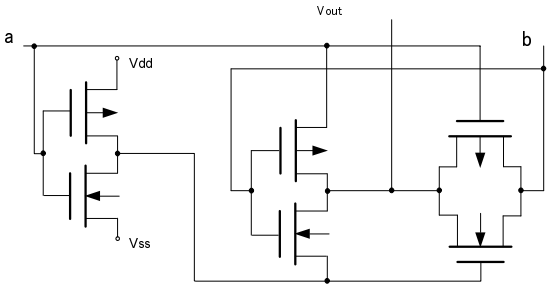

Fig. 3 New schematic for exclusive-OR CMOS.

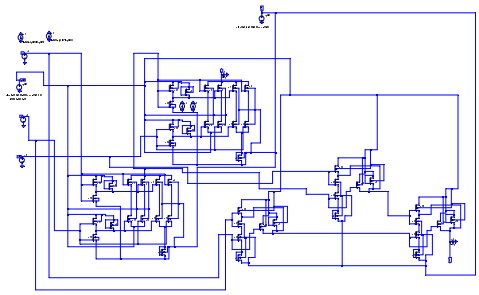

Fig. 5 Schematic of full adder 2PASCL.

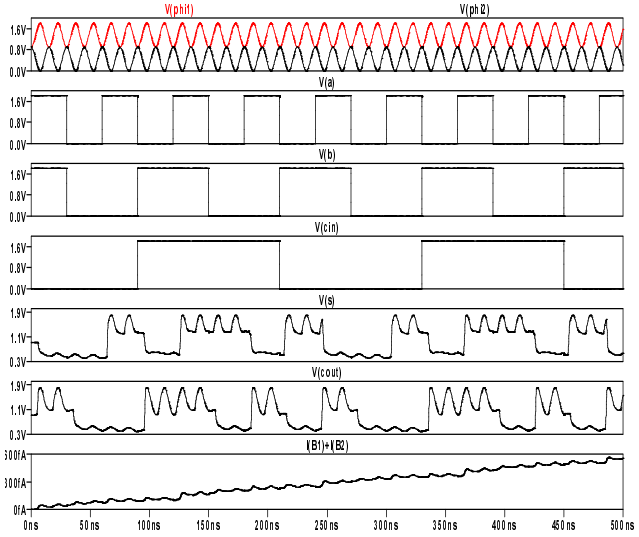

Fig. 6 Waveforms for full adder 2PASCL from the simulation result.

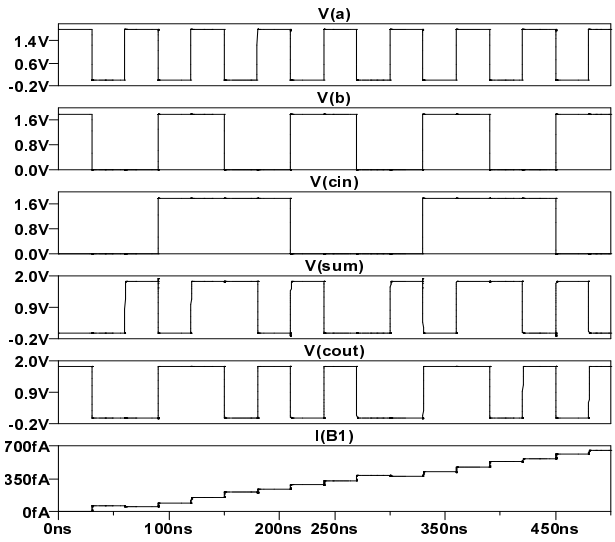

Fig. 7 Waveforms for full adder CMOS from the simulation result.

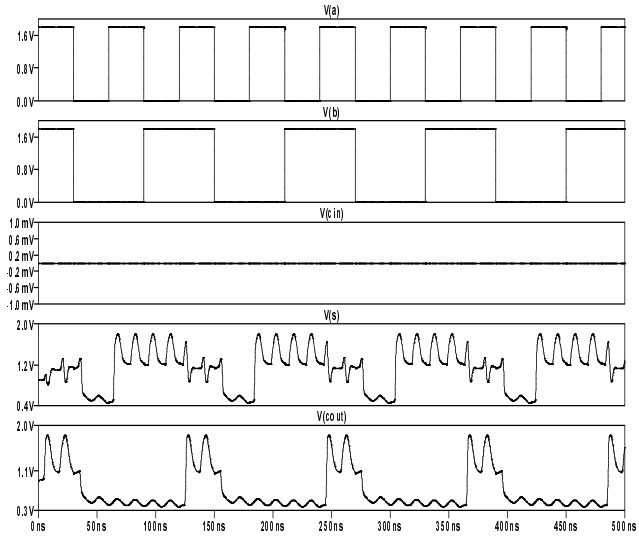

Fig. 9 Waveforms of ripple carry adder (RCA) 2PASCL from the simulation result.