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# Ultra low power and fast tuning interpolator in digital controlled oscillator for all digital phase locked loop

**Syaza Norfilsha Ishak[1,3] · Jahariah Sampe[1,3] · Nazrul Anuar Nayan[2,3] · Huda Abdullah[2,3] · Noor Hidayah Mohd Yunus[4] · Mohammad Faseehuddin[5]**

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**Abstract**
All-digital phase-locked loops (ADPLL) have become increasingly attractive to academicians and industries in system-on-chips applications due to advancements in complementary metal-oxide-semiconductor (CMOS) technology, particularly in terms of reduced power consumption and smaller chip area. In ADPLL, the most vital component is the digital oscillator design, which comprises a coarse-tuned part and a fine-tuned part. This work focuses specifically on the fine-tuning part to enhance the power dissipation performance of the digital oscillator in the ADPLL. The interpolation technique is employed in circuit design, utilizing two types of controllable inverter configurations with proper sizing of CMOS within a single stage. The interpolator fine-tuned circuit consists of seven stages and is controlled by a 6-bit phase control input. This design achieves a phase step of 6 ps to 31 ps, with a power dissipation of 0.09 $\mu$W at a supply voltage of 1.2 V. The circuit is implemented using the Silterra 130 nm technology process, and the post-layout design achieves a compact dimension of 0.00789 mm$^2$.

**Keywords** Digital interpolator · Phase interpolator · Fine tuning · DCO · ADPLL

## 1 Introduction

During the last decade, the transition from analog to digital has become increasingly complex due to the advancement of CMOS technology in microprocessors and system-on-chips (SoCs) [1–4] and the phase-locked loop (PLL) is one application that has not been missed. The traditional PLL consists of analog components, mainly a support circuit known as a frequency synthesizer, to produce a comprehensive and stable varying high-frequency range for the local oscillator (LO) in the transceiver. However, the aim of ultra-low power with wider frequency, high-speed system, better phase noise performance, compact chip area, and low-cost requirement of the RFID [5] make the realization of traditional analogue PLL irrelevant.

Jahariah Sampe, Nazrul Anuar Nayan, Huda Abdullah, Noor Hidayah Mohd Yunus, Mohammad Faseehuddin have contributed equally to this work.

✉ Jahariah Sampe
jahariah@ukm.edu.my

Syaza Norfilsha Ishak
syazanorfilsha@gmail.com

Nazrul Anuar Nayan
nazrul@ukm.edu.my

Huda Abdullah
huda.abdullah@ukm.edu.my

Noor Hidayah Mohd Yunus
noorhidayahm@unikl.edu.my

Mohammad Faseehuddin
faseehuddin@thapar.edu

[1] Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia, Bangi 43000, Selangor, Malaysia

[2] Department of Electrical, Electronic and Systems Engineering, Faculty of Engineering and Built Environment, Universiti Kebangsaan Malaysia, Bangi 43000, Selangor, Malaysia

[3] Universiti Kebangsaan Malaysia, Bangi 43000, Selangor, Malaysia

[4] Communication Technology Division, Universiti Kuala Lumpur British Malaysian Institute, Gombak 53100, Selangor, Malaysia

[5] Thapar Institute of Engineering and Technology, Patiala 147004, Punjab, India

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A digital controlled oscillator (DCO) is a vital component in ADPLL and an important block, the same as the voltage-controlled oscillator (VCO) in PLL. It generates a controllable tuning frequency range with a precision technique for the system's LO. It also can be performed in an LC tank-based oscillator [6–8] or a delay ring-based oscillator [9–11]. This DCO is the most essential part because the output frequency directly impacts the timing accuracy where phase alignment is required and the signal-to-noise ratio (SNR) frequency translation is performed [12]. This output frequency will affect the design's jitter and phase noise performance and the circuit's power consumption.

With the extensive high-speed applications in RFID, a wide range of oscillators is needed to operate at lower power consumption with smaller chip sizes. Almost all VCOs in analog PLLs and mixed-analog-digital reported in the literature [13–19] are designed with inductor (L) and capacitor (C) banks to operate the tuning frequency. The LC factor can be increased to achieve good power performance and better phase noise results. However, increasing the LC factor may lead to a large area. For these reasons, digital oscillators are preferred over analog ones, and the ring-based oscillator type is chosen to be discussed. This is because the delay ring type behavior is similar to the digital, and typical digital's CMOS processes do not provide high-quality inductors, which occupy a large area.

Ring oscillators (RO) are trending nowadays due to their non-complexity of design, wide range tuning frequency, low power performance, and small chip area. RO performed well not only in PLL but also in ADPLL. The frequency tuning step in DCO is built with two architectures: (1) Coarse tuning block and (2) Fine-tuning block, either for LC-DCO or ring-DCO. These tunings are needed to operate the DCO with better resolution. In RO, the inverter delay ring is performed as a coarse tuning block, and the phase shifter or interpolator is built as a fine-tuning block in DCO. Some works reported that their DCOs are built with only one block for coarse tuning and one block for fine-tuning [20–24], and some others reported that their DCOs need more than one fine-tuning step [25–27]. The different architectures of the coarse tuning and the fine-tuning are based on the target application.

The coarse tuning aims to set the initial oscillator's frequency so that it is often near the desired frequency. Meanwhile, fine-tuning makes more precise adjustments to achieve the desired frequency. Fine-tuning elements typically have a smaller tuning range and higher resolution than course-tuning elements. As a result, the design of the DCO is critical. Currently, the phase interpolator (PI) has evolved significantly in the DCO of high-performance ADPLL as the fine-tuning mechanism. The use of a phase interpolator for DCO fine-tuning lies in its ability to interpolate between discrete phase steps, effectively enabling high-resolution frequency adjustment without requiring excessive hardware complexity or high-power consumption. Unlike traditional frequency tuning methods that rely solely on coarse capacitors or varactor banks, which introduce large frequency steps, phase interpolators enable smooth phase transitions with minimal quantization noise. This is particularly beneficial in fractional-N phase-locked loops (PLLs), where fine-tuned phase adjustments are crucial for reducing in-band phase noise and fractional spurs. For example, in the hierarchical DCO with a 32-stage current-starved inverter-based phase interpolator [9], the design achieves 6 ps resolution, significantly improving frequency granularity without excessive power overhead. Similarly, in the retiming-based digital PI (DPI) of work [28], phase interpolation is used within a fractional frequency divider (FFD) to achieve sub-cycle frequency tuning, ensuring minimal phase jitter and better chirp linearity in FMCW radar applications.

Furthermore, current-steering and charge-sharing phase interpolators, as seen in the harmonic rejection phase interpolator (HR-PI) [29], provide enhanced linearity by suppressing harmonic distortion, improving signal purity in high-frequency applications. The inverter-based phase interpolator in [30] demonstrates another practical implementation, where quadrature phase interpolation achieves 4–5 ps resolution per step while minimizing power consumption. Such designs show that phase interpolators integrate efficiently into digital DCO architectures, allowing for fine frequency tuning without requiring high-resolution capacitor banks or complex varactor tuning circuits. Additionally, phase interpolators enable fast frequency switching, as seen in [29], where a phase interpolator-based divider enables precise sub-cycle interpolation, reducing lock time and jitter accumulation. The use of background calibration techniques in some designs further enhances the linearity and accuracy of phase selection, ensuring that DCO fine-tuning remains robust against process, voltage, and temperature (PVT) variations. Overall, the interpolator provides a balance of high resolution, low power consumption, and improved phase noise performance, making it a superior choice for fine-tuning DCOs in modern PLL architectures.

Despite improvements in phase accuracy, resolution, and spur suppression, phase interpolator designs still suffer from nonlinearity, PVT variations, and residual phase noise. One significant gap is the lack of an ultra-linear, low-power PI architecture that maintains resolution below 5 ps without significant power overhead. Most existing solutions rely on inverter-based or current-steering architectures, which trade linearity for power efficiency or require complex calibration techniques. Furthermore, interpolators that rely on discharge switches or charge-sharing techniques introduce settling time delays, limiting their usability in high-speed, high-frequency PLLs. To bridge these gaps, a low-power,

high-linearity phase interpolator with PVT robustness, and minimal phase noise are required to improve fine-tuning capabilities in DCO-based frequency synthesis.

In this work, the optimized CMOS tri-state-based inverter of the phase interpolator is proposed to improve the previous PI performance that will align with the target of the delay ring oscillator application. Choosing the proper size of width (W) over length (L) W/L of the CMOS inverter in 130 nm technology will reduce power consumption and improve the linearity performance without PVT consideration. In order to achieve a maintained resolution below 35ps to 6ps with operating frequencies ranging from 500 MHz to 2.5 GHz, respectively, a 64-step architecture will be designed in the proposed phase interpolator.

## 2 Phase interpolator as the fine-tuning for the DCO

Figure 1 shows the architecture of the target DCO module for this work. It consists of a DCO decoder, a ring oscillator (RO) for coarse tuning, and a phase interpolator for fine-tuning. The DCO decoder receives the codeword from the other ADPLL block, which is the controller, and processes it to vary the frequency in the RO and the phase interpolator. The RO's role is to vary the large step size near the target frequency, and the phase interpolator will adjust the small step size to achieve the target frequency to design a high-speed application.

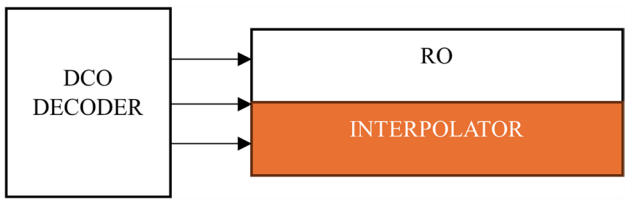


**Fig. 1** Proposed DCO module

Phase-interpolators have been used in applications such as polar modulation circuits in wireless transceivers, phase-locked loops (PLL), Clock and Data Recovery (CDR), and delay-locked loops (DLL) for adjusting the phase of the sampling clock [31]. Various techniques have been proposed that use multi-phase to improve circuit performance [32].

Generally, a phase-interpolator (PI) concept is a circuit that generates a new output clock signal with a phase between two input clock signals with different phases, as illustrated in Fig. 2. It consists of weights or amplitude coefficients labeled as $K_1$ and $K_2$. These weights can be positive, negative, or zero for input signals, allowing various combinations and phase shifts. The interpolated signal for two input summation is given by,

$$K_{PI}Sig_{PI}(\omega_t + \theta_{out}) = K_1.Sig_1\theta_1 + K_2.Sig_2\theta_2 \quad (1)$$

$$= \sqrt{K_1^2 + K_2^2}.Sig_1(\omega_t + \theta_{out}) \quad (2)$$

where $K_{PI} = \sqrt{K_1^2 + K_2^2}+$ is the gain of the PI and $\theta_{out} = \tan^{-1}(\frac{K_2}{K_1})$ is the phase of the interpolated signal. In order to ensure the monotonicity and linearity of the PI, the gain $K_{PI}$ should remain constant [31]. In the DCO, PI allows for excellent adjustment to the phase of a clock signal and provides a finer level of phase adjustment, enabling more precise frequency control. It can also be known as a phase shifter.

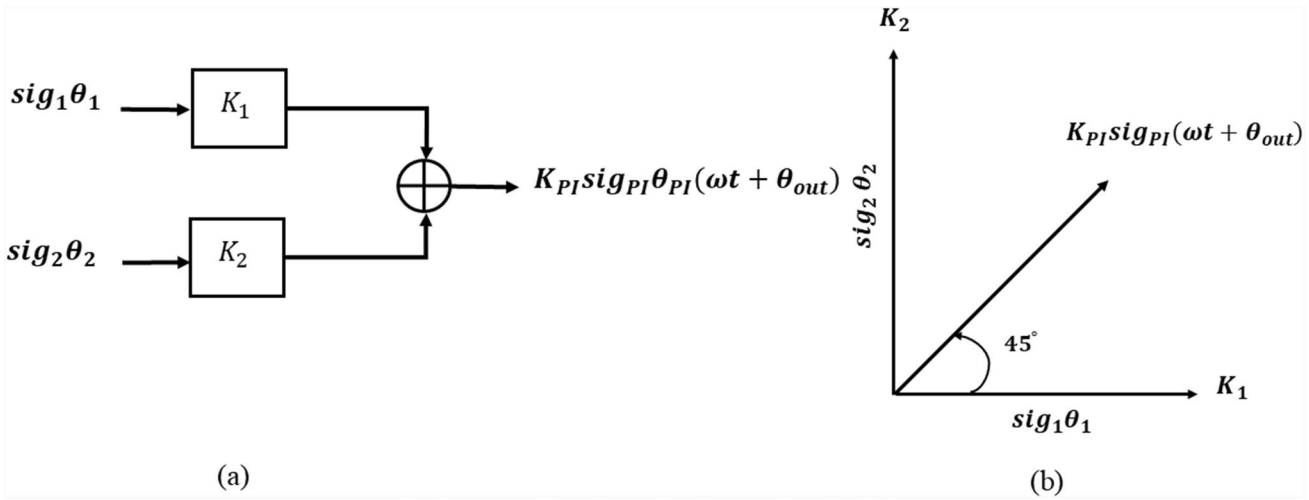


**Fig. 2** General phase shifter concept **a** the summation of two signals with phase **b** the magnitude and direction of the interpolator output

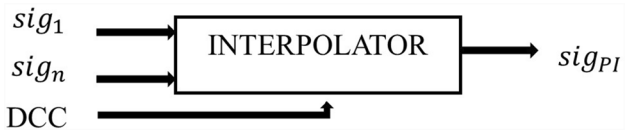


**Fig. 3** Interpolator block diagram system

Figure 3 shows the block diagram of the PI for this work, where the $Sig_1$ is referred to as the first input clock with phase, the $Sig_n$ is as the nth input clock with phase, the $Sig_{PI}$ is the output clock signal with total phase, and DCC refers to the digital control code. The DCC is employed to control the selected interpolator switches in the circuit, allowing the output signals to be generated as needed by the system.

Figure 4 demonstrates the summation concept for this work of PI and its characteristics of phase control code (DCC) in bit vs. PI phase out ($\theta_n$).

## 3 Traditional phase shifter

The phase interpolator or phase shifter is traditionally built from the inverter delay chain, as shown in Fig. 5. An inverter is an essential digital logic gate that performs the NOT operation. It takes a single input bit and produces the opposite output. In simple terms, if the input is 1, the output is 0, and vice versa. While inverters are primarily used for logic operations, they also introduce a delay to signal passing through them. This delay is mainly due to propagation delay and internal switching delay. When inverters are connected in series, they form a delay line. Each inverter adds its propagation delay and switching time to the total delay of the signal. Therefore, the overall delay of the signal passing through the series of inverters is the sum of the individual delays of each inverter.

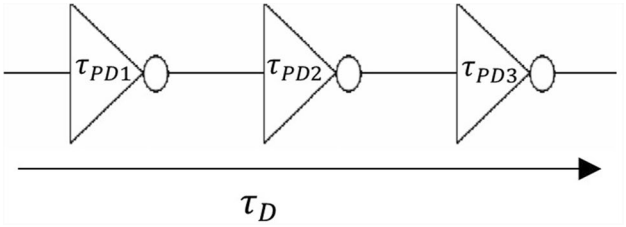


**Fig. 5** Traditional phase shifter

In Fig. 5, each inverter represents a delay element as the signal travels from left to right. The total delay $\tau_{PDtotal}$ experienced by the signal is the sum of the delays introduced by all the inverters and can be expressed as follows.

$$\tau_{PDtotal} = \tau_{PD1} + \tau_{PD2} + \tau_{PD3} \tag{3}$$

However, the propagation delay inherent in each inverter can be defined as the mean of the delay values of the rising edge's low-to-high ($\tau_{plh}$) and falling edge's high-to-low ($\tau_{phl}$) transition and it is elaborated in a particular formula as follows.

$$\tau_{PD} = \frac{\tau_{phl} + \tau plh}{2} = 0.69 C_L \frac{R_{eqN} + R_{eqP}}{2} \tag{4}$$

While the total output capacitance ($C_{out}$) is defined in the circuit as:

$$C_{out} = C_{DN} + C_{DP} + C_L \tag{5}$$

where $C_{DN}$ and $C_{DP}$ are internal capacitance values produced by the NMOS and the PMOS transistors, respectively. While $C_L$ is the capacitance value at the load of the circuit.

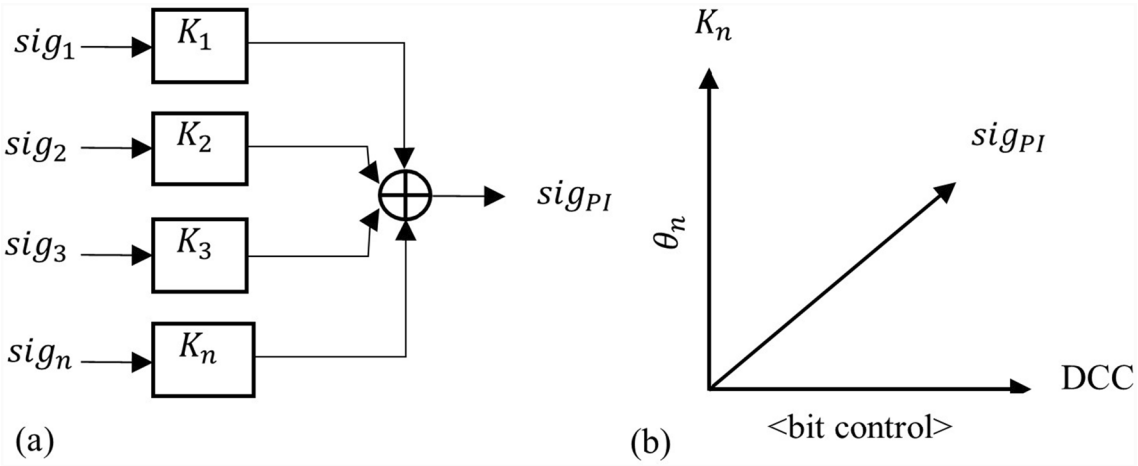


**Fig. 4** **a** Summation of PI **b** phase control code for n vs phase output

On top of that, according to the works of literature, the performance of the inverter's propagation delay can be influenced by the width over length (W/L) ratio of the transistor. This ratio is formally defined as the rate of the ratio between the drain current and the carrier mobility in a fundamental MOS device [33]. With some modifications to the value of the W/L ratio, the delay will be adjusted and other performances such as switching frequency also will be enhanced. Besides that, based on the mathematical analysis, the delay also introduced by an inverter depends on other factors, including manufacturing technology (CMOS tech.), supply voltage variation, temperature variation, and load capacitance.

In digital circuits, phase shift refers to the time difference between two signals. When a signal is delayed relative to another, it is said to be phase-shifted. As discussed earlier, an inverter chain introduces a delay to the signal passing through it. The simulation on the traditional phase shifter of six inverters has been conducted, and it is connected in a series chain. By tapping into different points along this chain, we can obtain signals with varying phase shifts relative to the original input signal. Figure 6 shows the simulation result for the traditional phase shifter with six inverters. The result indicates that the total phase shift on Tap_3 is thrice that from the first tapping point (Tap_1). This is because the total propagation delay on Tap_3 is larger than the others. This also shows that the amount of phase shift depends on the number of inverters between the tapping points. Thus, this simulation proved the equations (2) and (3).

## 4 Phase interpolator design consideration

A controllable inverter-based whose delay can be dynamically adjusted and acted as a digital logic gate. This control can be achieved using various techniques, such as variable supply voltage that influences switching speed, variable transistor dimensions by adjusting the width and length of the transistor, and variable delay cell, which consists of incorporating delay cells within the inverter.

A general mathematical model for the controllable inverter delay can be expressed as:

$$\tau_{PD} = f(VDD, W, L, D) \tag{6}$$

VDD is the supply voltage, W and L are the width and length of the transistor, respectively, and D is a control parameter.

1. Assuming a linear relationship between delay and supply voltage are given below.

$$\tau_{PD} = K_1 * VDD^{\alpha} \tag{7}$$

2. A common model for transistor delay is represented as follows.

$$\tau_{PD} = K_2 * (\frac{W}{L})^{\beta} \tag{8}$$

,where $\alpha$ and $\beta$ are the CMOS technology process-dependent constants.

3. The delay of a variable delay cell can often be modeled as a linear function of the control signal and given as:

$$\tau_{PD} = K_3 * D \tag{9}$$

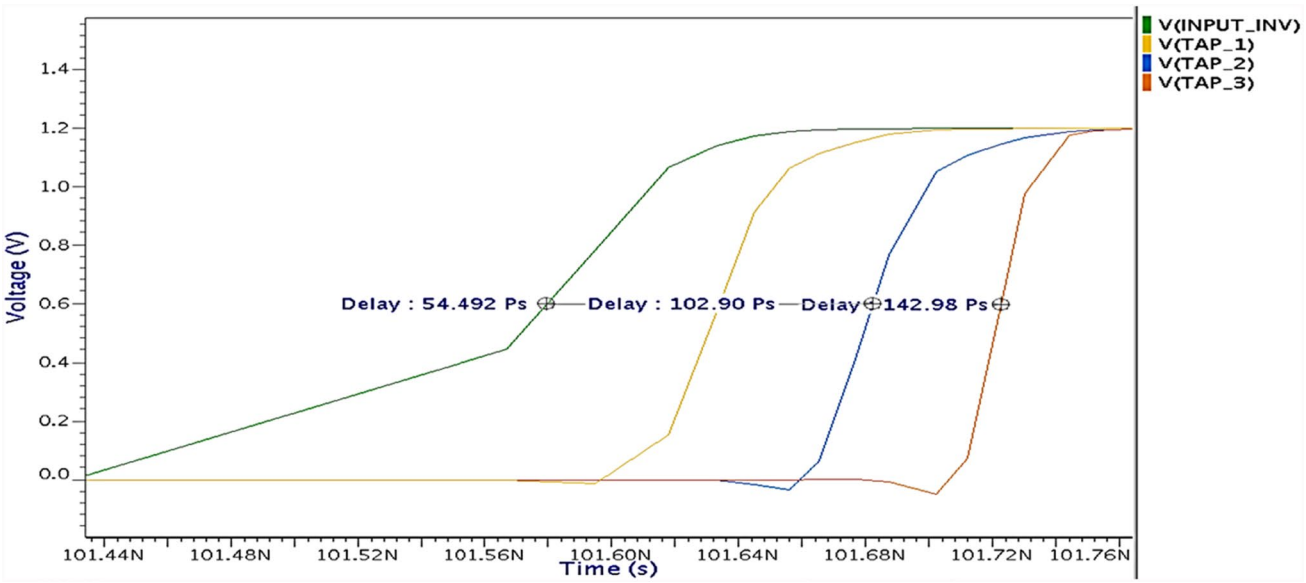


**Fig. 6** The simulation of the traditional phase shifter for Tap_1, Tap_2, and Tap_3

For a controllable inverter that uses a combination of the techniques, the total delay can be modeled as:

$$\tau_{PD} = K_1 * VDD^{\alpha} + K_2 * (\frac{W}{L})^{\beta} + K_3 * D \quad (10)$$

,where $K_1$, $K_2$, and $K_3$ are the weight coefficients for each techniques.

In addition, assume the inverter chain has N inverters. Each inverter has its delay $\tau_{PD}$. The input frequency is defined as $f_{in}$. For a single controllable inverter, the phase is defined as:

$$\emptyset_{inv} = 2\pi * \tau_{PD} * f_{in} \quad (11)$$

Hence, for the N-chain inverter, the total phase can be calculated as:

$$\emptyset_{N\_inv} = N * \emptyset_{inv} \quad (12)$$

In this case, the controllable inverter is arranged in the traditional configuration as in Fig. 5 with six stages and the phase shift is shown in Fig. 7.

The waveforms in Figs. 6 and 7 illustrate the propagation delays of different phase shifts by using an inverter and tri-state inverter, respectively in a traditional configuration shifter circuit. Figure 6 exhibits lower delay values of 54.492 ps, 102.90 ps, and 142.98 ps, whereas Fig. 7 shows increased delays of 121.18 ps, 214.18 ps, and 272.35 ps, along with more gradual transitions, suggesting higher resistive or capacitive effects. The reduced propagation delay in Fig. 6 makes it more suitable for faster phase interpolation, improving phase resolution and reducing timing jitters in high-speed applications. In contrast, the smoother transitions in Fig. 7 may enhance phase accuracy and reduce noise, making it preferable for target applications to prioritize linearity and stability. However, with proper sizing of the CMOS transistor for tri-state configuration, the propagation delay can be decreased, and the phase interpolation speed can be fast.

### 4.1 Inverter as main component

Inverters are essential parts of the interpolators for this work, and factors such as high resolution, fast switching speed, low noise, and good precision in timing control must be considered. In this work, high-speed CMOSFET-based inverters are selected. This inverter type is chosen due to its fast-switching characteristics, low resistance, and high-efficiency advantages. However, minimizing the parasitic effects when designing the layout is challenging. Thus, a careful layout design must be considered.

This work designs a new configuration of the tri-state inverter-based for high-speed interpolator applications with proper sizing of CMOS. It aims to provide a comprehensive overview of critical considerations, including the switching frequency, the delay, and the power dissipation. The simulation for this work is set up with characteristics of CMOS technology using Silterra 130 nm process, and the PMOS/NMOS transistor size ratio indicates ranging from 2.5/1 to 3/1 while the voltage supply is 1.2 V.

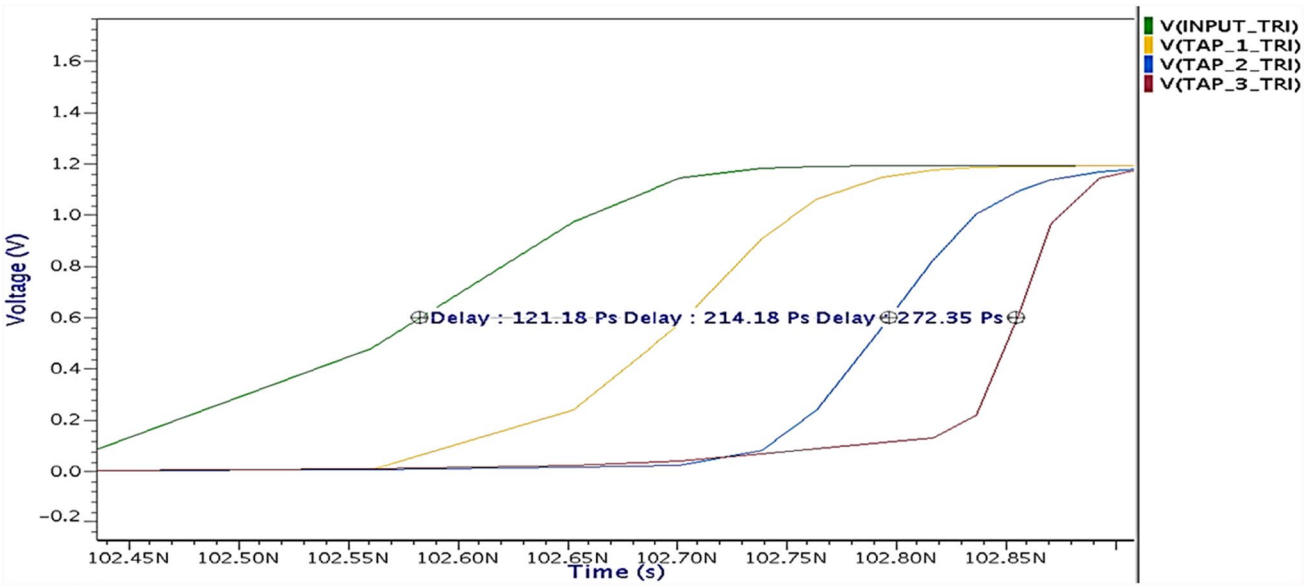


**Fig. 7** The simulation of the traditional phase shifter by using controllable inverter

### 4.2 One stage interpolator with controllable inverter configuration

Figure 8 shows the traditional configuration circuit built with a controllable tri-state inverter as in [9]. In this configuration, one stage of the interpolator uses two inverters of the same type. This circuit performance can produce 32 steps of phase interpolator. However, the stage construction is very large, which requires 32 stages and the enable inputs of En1 and En2 require different input signals. This leads to high power consumption and large area of the design.

In this case, the control parameter of D is set up as 2 bit, VDD = 1.2 V, the stage N = 2 and the technology used is 130 nm. Figure 9 shows the interpolated result for the traditional controllable inverter that is arranged as a phase interpolator at one stage. The green line waveform in Fig. 9 is the reference clock signal, which refers to the clock 0°, and the red line waveform is the quadrature-phase clock, which refers to the 90° out of phase with the reference. The next blue line waveform in Fig. 9 represents the 1-bit digital control, and the last line waveform shows the interpolated signal for this case. When the control bit changes from 0 to 1, the

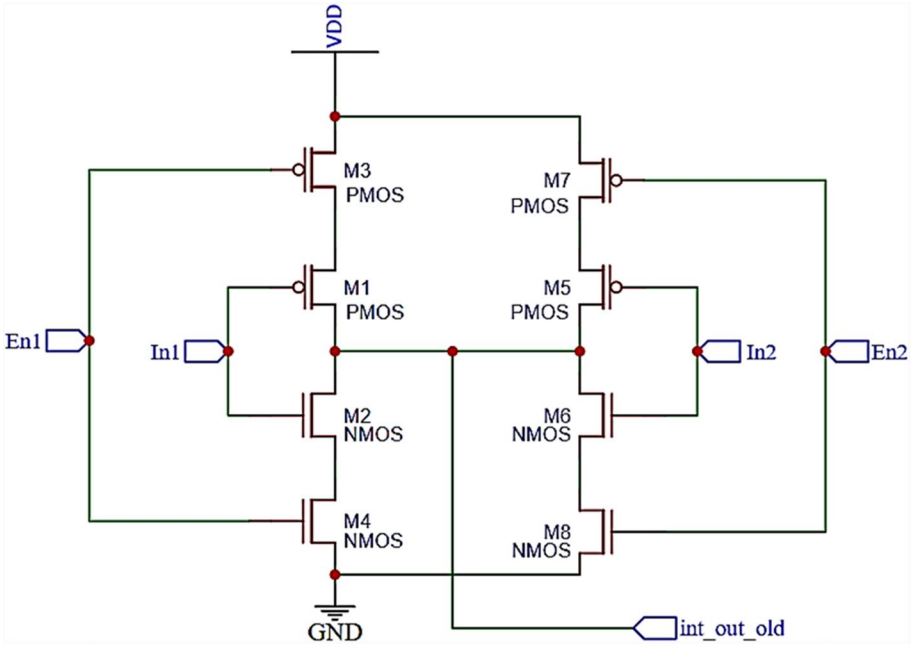


**Fig. 8** Traditional configuration of phase interpolator at one stage

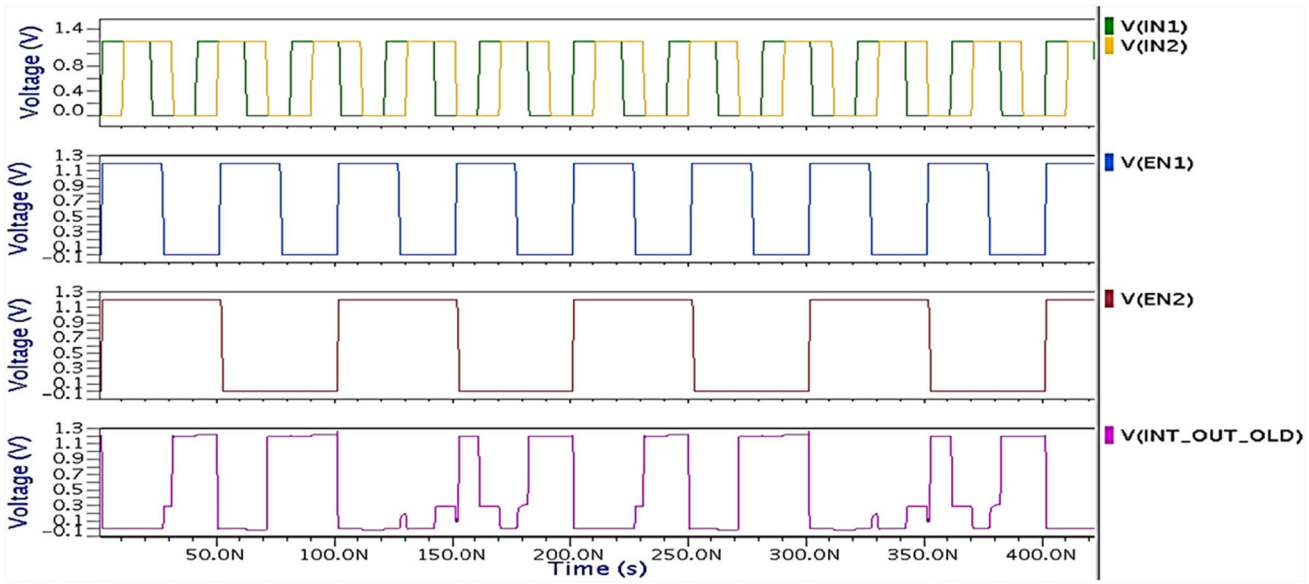


**Fig. 9** The interpolated result by using the traditional controllable inverter

interpolated output phase shifts accordingly. The resolution of phase control depends on the 1-bit digital input, allowing for $2^1 = 2$ discrete phase steps only. In order to increase the phase resolution, the control bits of D can be increased.

Figure 10 shows the new configuration of the phase interpolator at one stage. This configuration uses two types of controllable inverters as shown in Fig. 10a and b, to produce a complete phase interpolator for one clock cycle. The difference between the two types is that the controllable inverter in Fig. 10a has an extra pair of CMOS at the input to form the inverse function.

In comparison, the waveform in Fig. 9 demonstrates a traditional configuration phase interpolator utilizing two distinct enable signals, V(EN1) and V(EN2), which results in an output, V(INT_OUT_OLD), characterized by instability and noticeable glitches. In contrast, the revised configuration phase interpolator of the waveform in Fig. 11 incorporates a single enable signal, V(EN), leading to a significantly improved output, V(OUT_INT_NEW), with enhanced stability and reduced signal irregularities. This modification suggests an optimization in the enable control mechanism, contributing to improved interpolation accuracy and a more predictable output response.

Figure 12 shows the delay in performance for the one-stage interpolation circuit. The circuit exhibits a delay of 138.32 ps only from the input signal at a supply voltage of 1.2 V. While the switching voltage performance as shown in Fig. 13 for this work can be performed as fast switching at 532.53 mV. The circuit for one-stage interpolation also consumes 0.002255 $\mu$W at the same supply voltage

## 5 The proposed architecture of phase interpolator design

The architecture of the proposed phase interpolator is presented in Fig. 14. It consists of seven stages, each comprising a pair of controllable inverters, as shown in Fig. 10.

This interpolator will receive two input signals and various enable-inputs, En1 [5:0] and En2 [5:0], from the second stage until seventh stage to activate the interpolator inverters for producing interpolation signals. The enable inputs at the first stage are connected to the VDD to eliminate the unwanted signal. The proposed phase interpolator is designed with proper sizing of the W/L ratio for each stage to produce a 64-step interpolation result, which reduces power consumption and area.

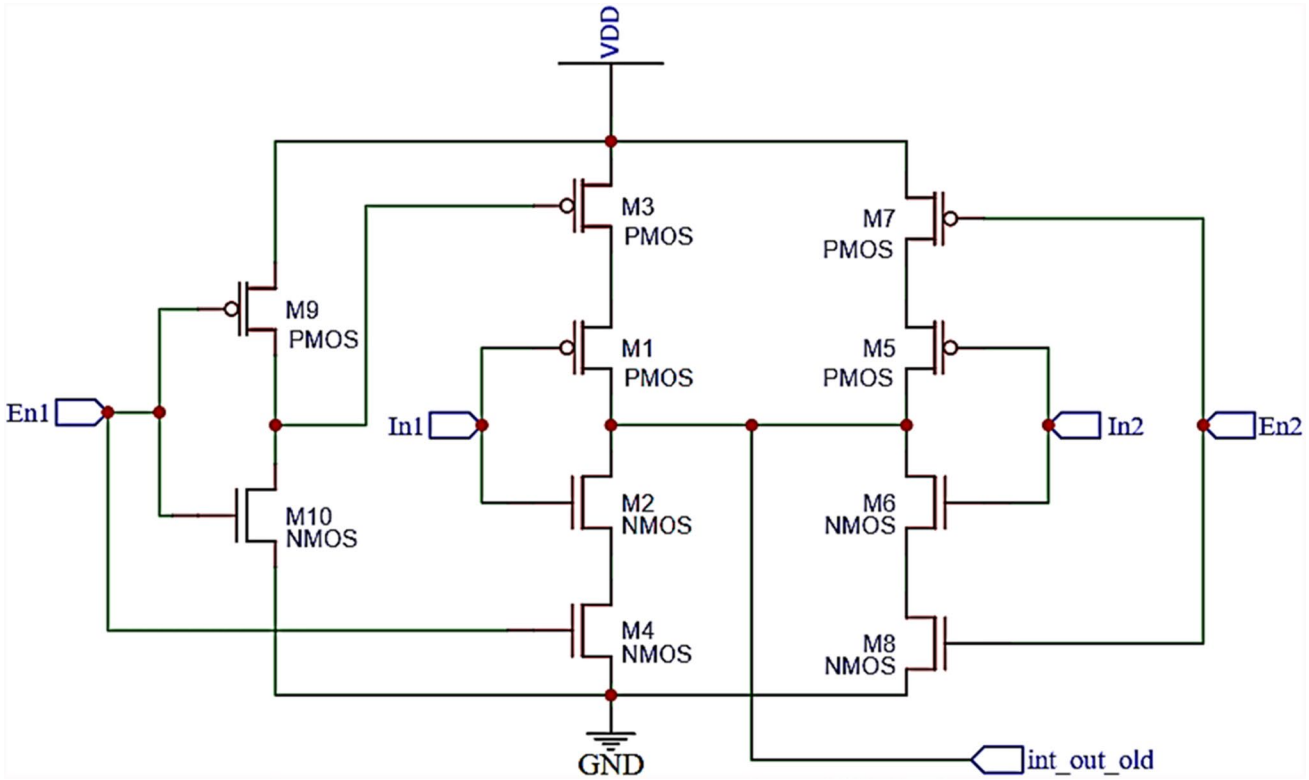


**Fig. 10** Two types of tri-state circuits **a** controllable inverter type-1 **b** controllable inverter type-2

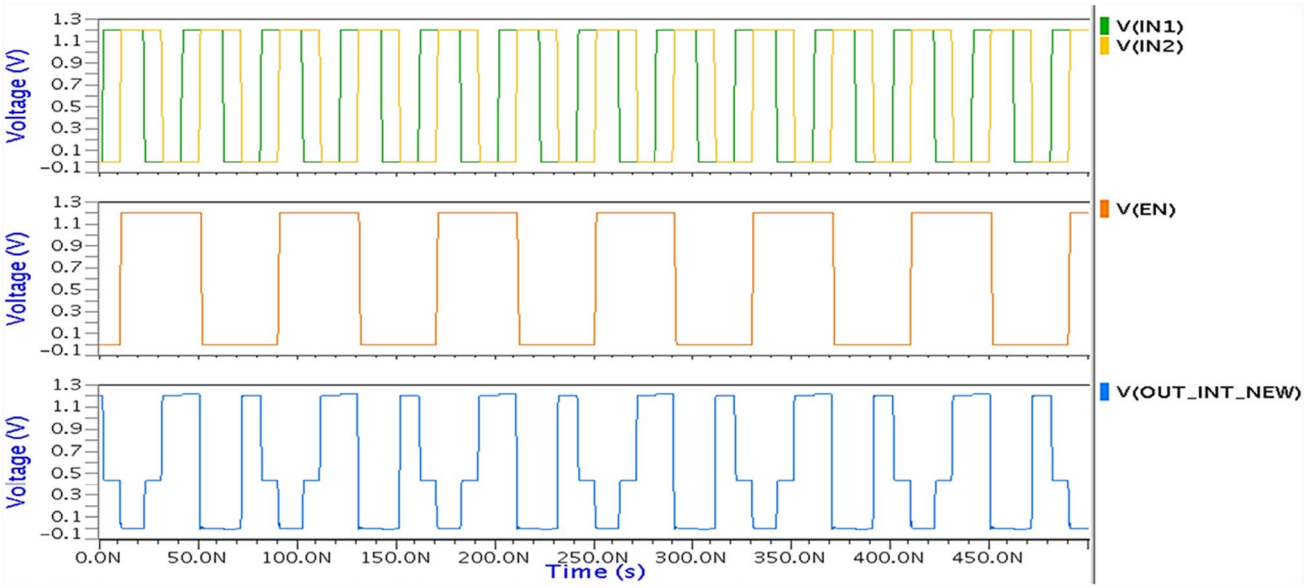


**Fig. 11** The interpolated signal at one stage

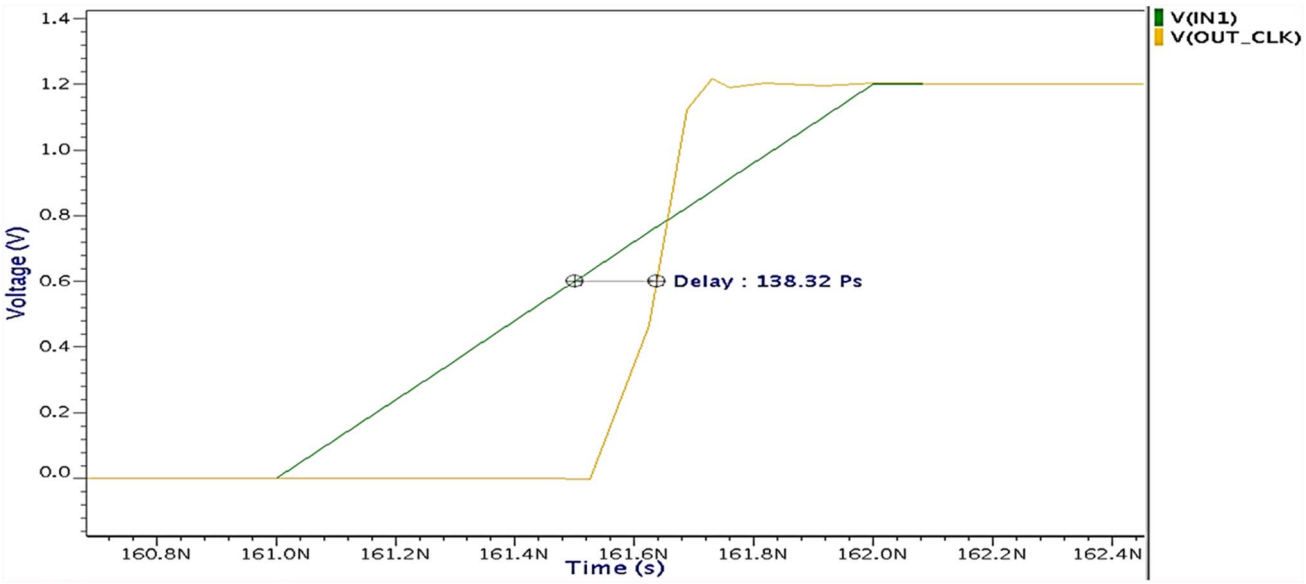


**Fig. 12** The propagation delay of the proposed tri-state configuration at one stage

## 6 Result and discussion

The proposed PI is designed and simulated in Mentor Graphics tools, employing 130 nm Silterra CMOS technologies under 1.8 V supply voltage. The layout of the interpolator is illustrated in Fig. 15. Its dimension is 44.41 $\mu$m × 17.77 $\mu$m, which occupies a very small area. The components of the PI stages are arranged according to the minimum distance or space required by the layout versus schematic (LVS) rule for the CMOS technology in order to achieve minimal performance reduction for the post-layout simulation. The total power consumption for this modification design is measured at 0.0578 $\mu$W and gets a good power reduction of 20% [21].

Figure 16 illustrates the result of the proposed phase interpolator for this work. The green waveform (V(IN1)) represents a high-frequency input clock and serves as the reference. The blue waveform (V(INT_CLK)) shows an interpolated clock signal, indicating phase shifting

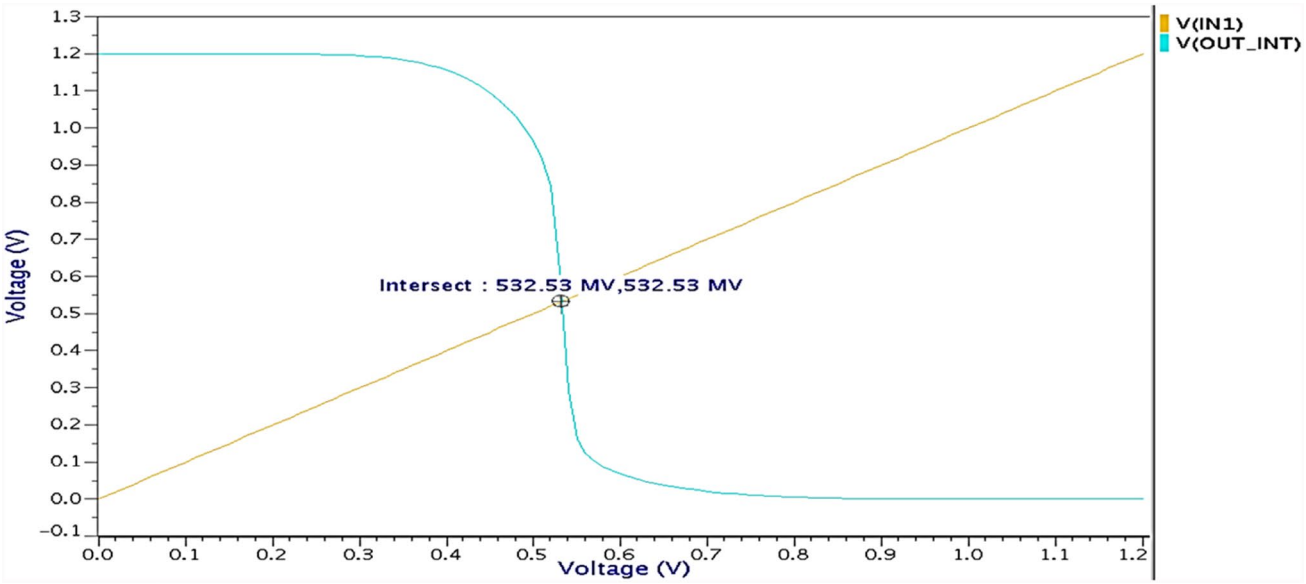


**Fig. 13** The switching voltage of the proposed tri-state configuration

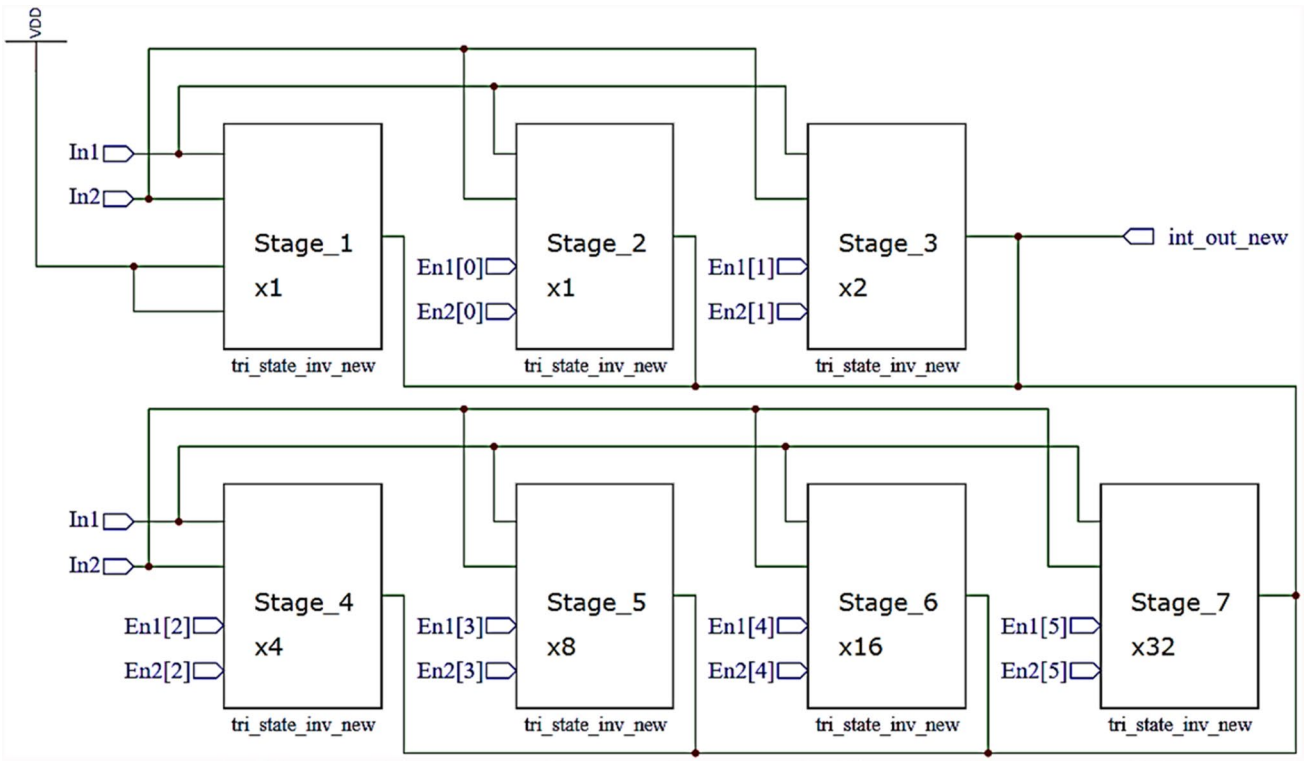


**Fig. 14** Proposed phase interpolator

or fine-tuned timing adjustments. The orange waveform (V(INT_OUT)) exhibits amplitude variations due to voltage-weighted summation that is controlled by bit D and the mixing of signal inputs 0° and 90°.

The corresponding phase step is selected by enabling a different number of inverters, and the delay performance of the interpolator is shown in Table 1. These performances are controlled by a set of enable and 6-bit phase controls. The

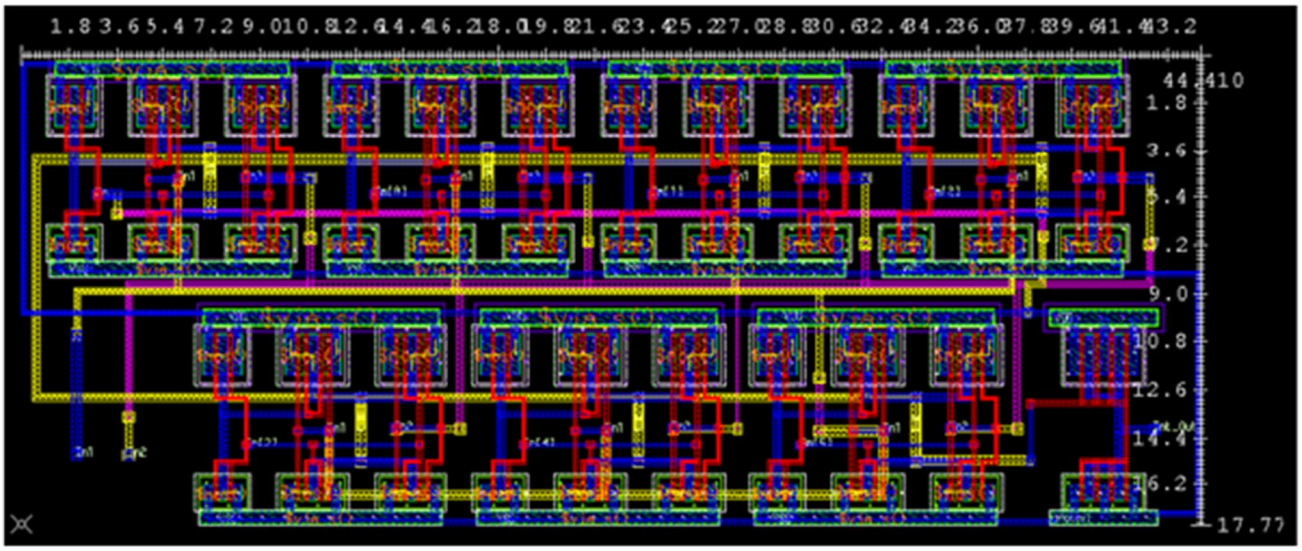

**Fig. 15** Layout of the proposed phase interpolator

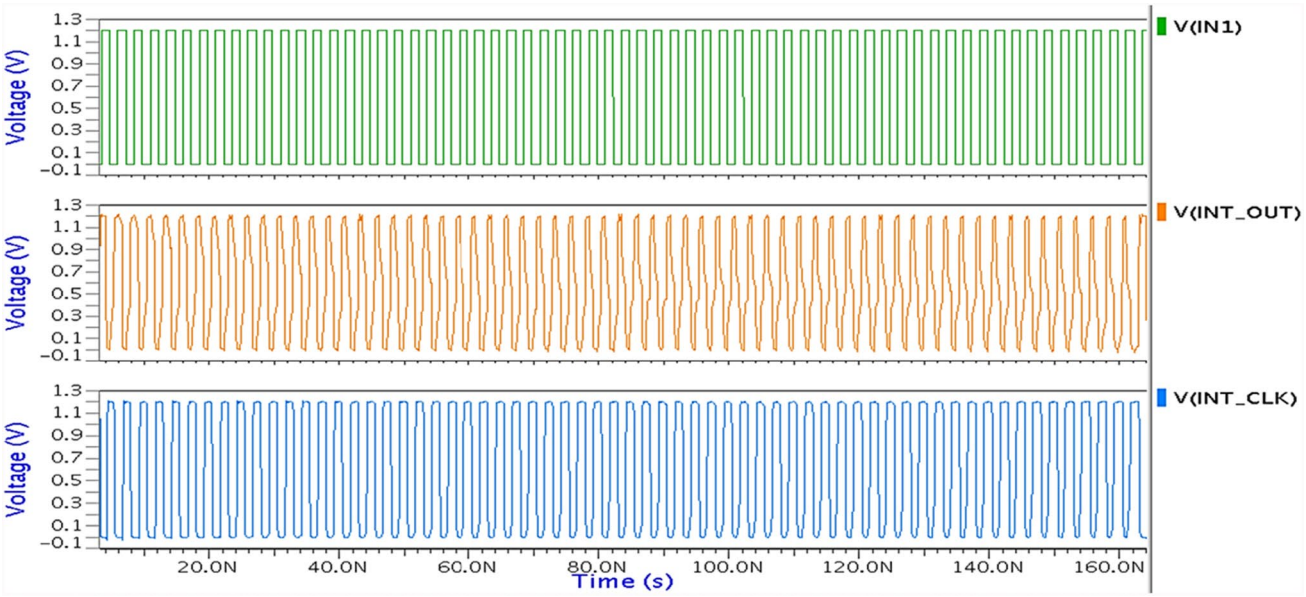


**Fig. 16** The result of the interpolated signal and phase shifting for the proposed interpolator

result shows that the delay increases when the bit control increases. This trend indicates that more delay stages are being bypassed. The phase step achieved in this design is between 31 ps to 1 ps which is deemed suitable for the fine-tuning of the DCO in future ADPLL applications.

The graph in Fig. 17 illustrates the relationship between delay time and bit control, where the delay time increases as the bit control value increases from 0 to 63. The different colored lines represent delays for different sizes of CMOS transistors of W/L ratio (2.5 to 3). Ideally, this should be a linear response, but the observed nonlinearity arises due to several factors. One key reason is an unequal weighting (K) of the inverters, where each inverter in the design does not contribute equally to phase adjustment due to circuit asymmetries and parasitic effects. Furthermore, supply voltage and process variations introduce additional non-idealities, as variations in power supply levels and semiconductor fabrication processes affect transistor performance, causing deviations from the expected linear delay behavior.

The comparison results in Fig. 17 show that higher W/L ratio values (2.75, 3) exhibit more stable and linear delay responses, while lower W/L ratios (2.5, 2.55, 2.6) show

**Table 1** Phase performance

| Enable inverter | Phase control bit | | | | | | Delay (ps) |
|---|---|---|---|---|---|---|---|
| | 0 | 1 | 2 | 3 | 4 | 5 | |
| Input | 0 | 0 | 0 | 0 | 0 | 0 | 631.4 |
| | 1 | 0 | 0 | 0 | 0 | 0 | 639.4 |
| | 0 | 1 | 0 | 0 | 0 | 0 | 643.59 |
| | 1 | 1 | 0 | 0 | 0 | 0 | 649.07 |
| | 0 | 0 | 1 | 0 | 0 | 0 | 651.7 |
| | 1 | 0 | 1 | 0 | 0 | 0 | 656.83 |
| | 0 | 1 | 1 | 0 | 0 | 0 | 658.93 |
| | 1 | 0 | 0 | 1 | 1 | 1 | 777.39 |
| | 0 | 1 | 0 | 1 | 1 | 1 | 784.14 |
| | 1 | 1 | 0 | 1 | 1 | 1 | 791.89 |
| | 0 | 0 | 1 | 1 | 1 | 1 | 801.06 |
| | 1 | 0 | 1 | 1 | 1 | 1 | 811.03 |
| | 0 | 1 | 1 | 1 | 1 | 1 | 822.44 |
| | 1 | 1 | 1 | 1 | 1 | 1 | 832.98 |

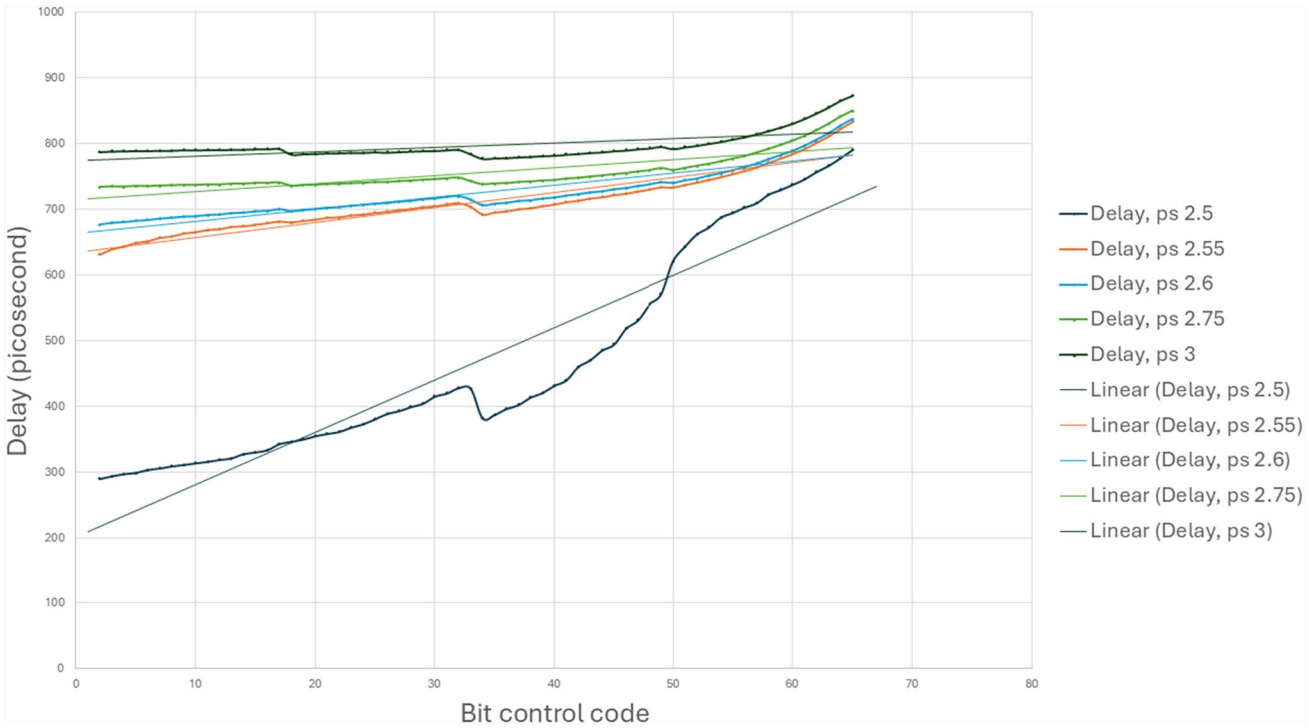


**Fig. 17** The trend line of phase delay corresponding to different transistor sizes of W/L ratios

noticeable nonlinearities and deviations from the expected trend. The W/L = 2.5 case, in particular, has significant variations, suggesting control granularity issues or circuit non-idealities. Higher W/L ratios provide a smoother and more predictable tuning range, whereas lower W/L ratios may introduce irregularities that affect fine resolution. Improving linearity at lower W/L ratios may require calibration techniques or circuit optimizations.

Table 2 presents a summary of the transistor sizing (Wp and Wn), supply voltage (VDD), and corresponding power dissipation for different PMOS-to-NMOS width over length (W/L) ratios (ranging from 2.5 to 3) in tristate inverters sizes in 130 nm that have been conducted in this work.

Figure 18 of the waveform illustrates the impact of these width ratios on signal transitions, highlighting differences in rise and fall times. As the ratio increases, the waveform

edges become steeper, indicating improved switching characteristics. This suggests that adjusting the transistor width ratio affects the drive strength, leading to variations in transition times and overall signal integrity. Additionally, the power dissipation values in Table 2 show a slight increase with larger width ratios, demonstrating the trade-off between switching speed and power consumption.

Table 3 compares the performance of this work with that of existing research. The comparison of phase interpolators across various references highlights key performance metrics, including technology node, supply voltage, number of interpolation steps, resolution, power consumption, and area. The proposed work demonstrates a significant reduction in power consumption at 0.09 $\mu$W, which is notably lower than

**Table 2** The summary of the transistor sizing in 130 nm technology by using proposed phase interpolator

| Stage (Bit Weight) | Tristate Inverter Sizes L=130 nm Technology | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| Ratio | 2.5 | | 2.55 | | 2.6 | | 2.75 | | 3 | |
| Transistor, $\mu$m | Wp | Wn | Wp | Wn | Wp | Wn | Wp | Wn | Wp | Wn |
| Connect VDD | 0.75 | 0.3 | 1.9125 | 0.765 | 1.95 | 0.78 | 2.0625 | 0.825 | 2.25 | 0.9 |
| $\mathbf{2^0}$ (LSB) | 2.5 | 1 | 6.375 | 2.55 | 6.5 | 2.6 | 6.875 | 2.75 | 7.5 | 3 |
| $\mathbf{2^1}$ | 4.5 | 2 | 11.475 | 5.1 | 11.7 | 5.2 | 12.375 | 5.5 | 13.5 | 6 |
| $\mathbf{2^2}$ | 8.5 | 4 | 21.675 | 10.2 | 22.1 | 10.4 | 23.375 | 11 | 25.5 | 12 |
| $\mathbf{2^3}$ | 16.5 | 8 | 42.075 | 20.4 | 42.9 | 20.8 | 45.375 | 22 | 49.5 | 24 |
| $\mathbf{2^4}$ | 32.5 | 16 | 82.875 | 40.8 | 84.5 | 41.6 | 89.375 | 44 | 97.5 | 48 |
| $\mathbf{2^5}$ (MSB) | 64.5 | 32 | 164.475 | 81.6 | 167.7 | 83.2 | 177.375 | 88 | 193.5 | 96 |
| Power ($\mu$W) | 0.09245 | | 0.09356 | | 0.09193 | | 0.0936 | | 0.095 | |

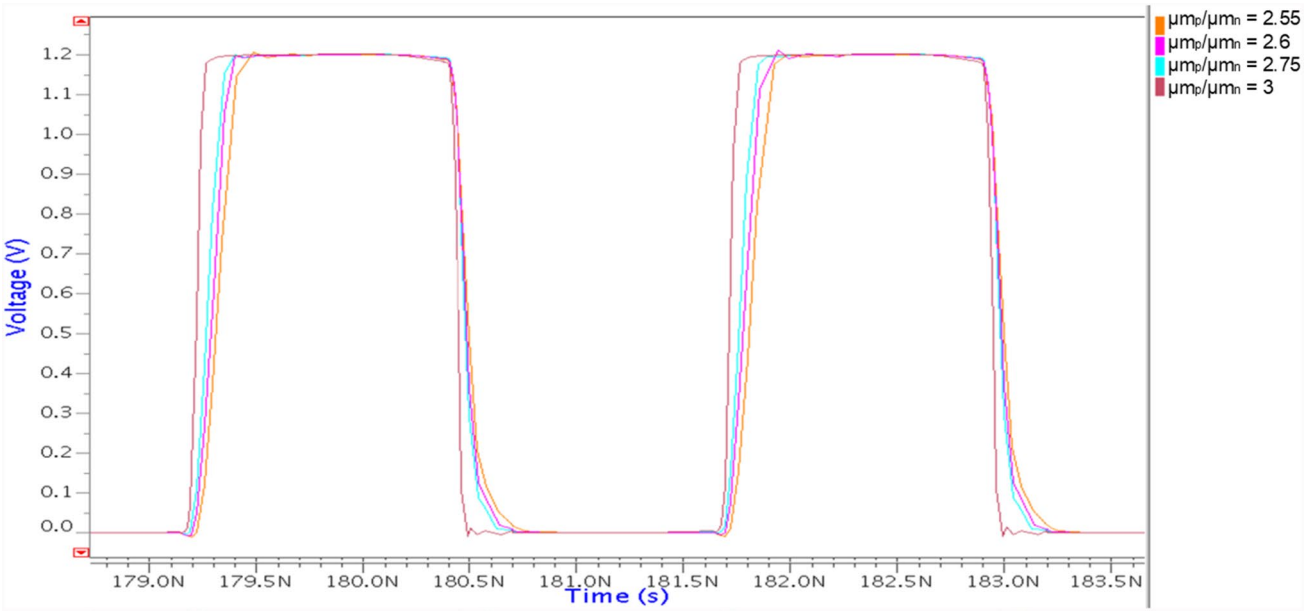


**Fig. 18** The impact of W/L ratios on signal transitions waveform

**Table 3** The comparison of the proposed design with other works

| References | Tech. (nm) | VDD (V) | Num. of steps | Res. (°) | Power (mW) | Area (mm$^2$) |
|---|---|---|---|---|---|---|
| [34] | 130 | 2.5 | 32 | 11.25 | 84 | 2.09 |
| [35] | 130 | 1 | 32 | 11.25 | 15 | n/a |
| [36] | 130 | 1.45 | 256 | 1.405 | 26 | 3.2 |
| [37] | 130 | 1.2 | 96 | 3.75 | <10 | 0.02 |
| This work | 130 | 1.2 | 64 | 5.625 | 0 | 0.00789 |

other references operating. Additionally, it achieves a compact area of 0.000789 $mm^2$, optimizing silicon utilization while maintaining competitive resolution and interpolation steps. The use of an advanced CMOS technology node further enhances efficiency, making the proposed design suitable for low-power, high-precision applications.

## 7 Conclusion

A seven-stage CMOS phase interpolator for high-speed application ADPLL is proposed in the paper. It is based on controllable inverter digital gates presenting a simple and flexible structure. It is designed to generate a programmable output phase with phases of 12.86°and 6-bit phase resolution and can be easily suited in a fine-tuning system for successive phase approximation. The topology is designed in a 130 nm CMOS process and offers 0.06 $\mu$W power consumption from a 1.8 V voltage supply. This PI also is occupied in a small area with a dimension of 44 $\mu$m × 17 $\mu$m. Hence, the performance of the proposed PI is achieved in order to be compliant with the high-speed interpolation of the DCO for the future ADPLL application.

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**Syaza Norfilsha Ishak** is a Master holder in Microelectronics Engineering from Universiti Kebangsaan Malaysia (UKM) and a Bachelor's degree holder in Electrical Engineering from Universiti Teknologi Malaysia (UTM). She had experience as Firmware Engineer at Creative Tech. Engineering Sdn Bhd and currently pursuing PhD in the Institute of Microengineering and Nanoelectronics (IMEN), Universiti Kebangsaan Malaysia (UKM). Her research interests are digital and analog circuit design, microcontroller programming, and microelectronics.

**Jahariah Sampe** is an Associate Professor and researcher at the Institute of Microengineering and Nanoelectronics, Universiti Kebangsaan Malaysia. With a PhD in VLSI design and a strong background in electrical, electronic, and system engineering, she specializes in areas such as Very Large Scale Integration (VLSI) design, digital and analogue circuits, energy harvesting using alternative resources, wireless and data communication, and microelectronics. Her extensive research portfolio includes projects such as ultra-low power RF transceivers for biomedical monitoring, MEMS-based RF energy harvesters, and smart card design implementations. With over a decade of teaching experience, she has served as a senior lecturer and section head at Universiti Kuala Lumpur

Malaysia France Institute, Bandar Baru Bangi. In addition to her academic roles, she has contributed to the professional community as an IEEE conference reviewer and auditor for quality evaluation systems. Assoc. Prof. Jahariah is a member of the Malaysian Society of Engineering & Technology (mSET) and the Board of Engineers Malaysia (BEM), reflecting her commitment to excellence in engineering education and research.

**Nazrul Anuar Nayan** an Associate Professor, senior lecturer and researcher at the Department of Electrical, Electronic and Systems Engineering, Faculty of Engineering & Built Environment, Universiti Kebangsaan Malaysia (UKM) with a strong background in biomedical signal processing, microelectronics, and IoT (Internet of Things). He obtained a PhD in Electronics and Information Systems Engineering from Gifu University, Japan in 2011 and pursued a two-year post-doctoral research program (2014–2016) at the Institute of Biomedical Engineering, University of Oxford, United Kingdom. With over 13 research projects as Principal Investigator and more than 65 publications, including three books, journal articles, and conference papers, Dr. Nazrul has made significant contributions to the fields of healthcare, digital circuit design, and wireless communications. His research interests are expanding into AI-embedded robotics, IoT, and drone block programming, where he actively trains students and educators in Malaysia and Indonesia, introducing them to cutting-edge technology for education and industry applications.

**Huda Abdullah** is an Associate Professor for Functional Nanomaterials in the Faculty of Engineering and Built Environment at the Universiti Kebangsaan Malaysia (UKM). Her research strength lies in the field of nanomaterials with a specialization in producing and synthesis of nanostructure materials for solar cell fabrication, bio-sensor, microstrip patch antenna, and various electronic devices.

**Noor Hidayah Mohd Yunus** is a Senior Lecturer at UniKL BMI and was appointed as the Head of Section for Communication Technology. She graduated with a B. Eng. (Hons) in Electrical Engineering and continued Master Degree in Telecommunication and Information Engineering and a Ph.D in Microengineering and Nanoelectronics. Currently, she has supervised 3 postgraduate students. She works on Climate change, RF energy harvesting, 5G communication systems and MEMS.

**Mohammad Faseehuddin** is an Assistant Professor in the Department of Electronics and Communication Engineering at Thapar Institute of Engineering and Technology, Patiala, India. He earned his Ph.D. in Analog Integrated Circuits Design from the National University of Malaysia in 2019. Prior to that, he completed his M.Tech in Electronics Circuits & Systems at Integral University, Lucknow, in 2014, and his B.Tech in Electronics & Communications Engineering at Integral University, Lucknow, in 2010. His research interests encompass analog integrated circuit design, artificial intelligence, and machine learning applications in VLSI systems. Dr. Faseehuddin has contributed to several peer-reviewed journals and conferences, serving as a reviewer and associate editor for various publications. He has also been involved in teaching and research activities, including serving as a resource person in workshops and conferences. His work reflects a commitment to advancing knowledge in the field of electronics and communication engineering.